Architectural Exploration of Network Interface for Energy Efficient 3D Optical Network-on-Chip

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I dedicate this dissertation to my loving wife, my daughter and my parents

Contents

Abstract

Electrical network-on-chip (ENoC) has long been considered as the technology to improve the bandwidth and the performance of the interconnects in multiprocessor systems-on-chip (MPSoCs). However, with the increase of the intellectual property (IP) cores integrated on a single chip, electrical interconnects are less and less suitable to adapt the bandwidth and latency requirements of the nowadays applications. In recent years, with low power consumption, low latency, and high data bandwidth properties, optical interconnect became an interesting solution to overcome these limitations. Indeed, Optical network on chip (ONoC) is based on waveguides and optical signals can be driven from source to destination with very low latency. But unfortunately, the optical devices used to built ONoCs suffer from some imperfections which introduce losses during communications. These losses (crosstalk noise and optical losses) are the very important factors which contribute to the energy efficiency and performance of the system. Furthermore, Wavelength Division Multiplexing (WDM) technology can help the designer to improve ONoC characteristics, especially the bandwidth and the latency. However, using the WDM technology leads to introduce new losses and crosstalk noises which negatively impact the Signal to Noise Ratio (SNR) and Bit Error Rate (BER). In detail, it can result in a higher BER and increases the power consumption and therefore reduces the energy efficiency of the optical interconnects.

In order to address these problems, we first model and analyze the optical losses and crosstalk in WDM based ONoC. The model can provide the analyzing of the worst case of loss and crosstalk with different parameters of optical ring network-on-chip. Based on this model, we propose a methodology to improve the performance and then to reduce the power consumption of optical interconnects rely on the forward error correction (FEC). We present two case studies of lightweight FEC with low implementation complexity and high error-correction performance under 28nm Fully-Depleted Silicon-On-Insulator

(FDSOI) technology. The results demonstrate the advantages of using FEC on the optical interconnect in the context of CHAMELEON ONoC. Secondly, we propose a complete design of optical network interface (ONI) which ic composed of the data flow allocation, integrated FECs, data serialization/deserialization, and the laser power driver. These different elements are presented in this manuscript. Rely on this interface, an energy efficiency allocation management can be supported at runtime due to the application demands. This runtime management of energy-performance can be integrated into the ONI manager through configuration manager which located at each ONI. Finally, the design of an ONoC configuration sequence (OCS) located at the centre of the optical layer is presented. By using the ONI manager, the OCS can configure ONoC at runtime according to the applications performance and energy requirements.

Keywords – Optical Network-On-Chip, Forward Error Correction, Optical Network Interface, Energy Efficiency, Design Space Exploration

Chapter 1

Introduction

Since several decades, Moore's law and International Technology Roadmap for Semiconductors (ITRS) forecasted that the number of transistors in an Integrated Circuit (IC) will double every 18 months. This increase now leads to the integration of hundreds of intellectual property (IP) cores into a single chip. In these multi-core parallel architectures, the data exchanges between cores can raise a major concern in overall system design: need for high performance interconnects for high data bandwidth communication. In this context, the design of on-chip interconnect plays a very important role for energy efficiency and performance of the overall system.

Electrical interconnects are the traditional candidate technology which can adapt to the application communication requirements. However, due to the characteristics of metal wire capacitance and inductive coupling [35], the increase in interconnect noise and propagation delay of global signals limits the overall system performance. Although a lot of effort has been made to solve these problems using many different interconnect architectures, until now, finding effective solutions to overcome these limitations remains a critical challenge.

New interconnects technologies such as three-dimensional (3D) stacking and optical interconnects could be a key solution for future on-chip interconnects. Nanophotonics interconnects are considered as one of the promising technologies, which is a key for the design of such next-generation of multi-processor system-on-chip. Optical interconnect allows for the increase of bandwidth as well as the reduction of noise, latency and power consumption. Another approach to improve the power and the performance of system

performance is 3D-stacked technology. Indeed, 3D stacking is a new technology that stacks many silicon wafers or multi-layers and interconnects vertically by using Through Silicon Vias (TSVs). This technology can improve the performance of a system in terms of power consumption, interconnection length and footprint. However, the combined use of 3D stacking and Optical Interconnect (OI) does not completely ensure overall performance. Instead, the exploration in terms of energy efficiency and performance, as well as the trade-off between Electrical-Optical exchanges, must be studied in this context.

1.1 Context of 3D Optical Network-on-Chip

1.1.1 Optical Interconnect Technology

Photonics links have been often used from long distance communication to off-chip interconnects such as rack to rack, board to board, chip to chip or data central networks [104, 103, 23]. But since a couple of years, Silicon photonics seems to be a very interesting emerging technology for the integration of NoC on Multi-Processor System-On-Chip (MPSOC). This technology is based on the use of an optical wave-guide medium to transport optical signals from source to destination with a very short latency.

The key of this technology is the ability to use Complementary Metal-Oxide Semiconductor (CMOS) fabrication in larger-scale. Compared to electrical interconnects, the advantages of this technology are the reduction of crosstalk, the high bandwidth immunity to electromagnetic interference (EMI) and the potential lower power consumption.

These advantages can make optical technology becoming a promising technology to solve the problems of the electrical links.

Figure 1.1 illustrates the latency and energy efficiency of electrical and optical interconnects as a function of distance between source and destination nodes. The data are extracted from ITRS[1] for a 16nm SOI technology. As we can see in this figure, the dotted lines present the potential of optical links compared to the electrical links (solid lines). For future multi-core processors, this evolution can offer the possibility to replace electrical links by on-chip optical links. By using this technology, the power consumption can

[1] See http://www.itrs2.net/2011-itrs.html

be reduced and the bandwidth can be adapted to the requirements of data exchanges between a large number of cores in a single chip.

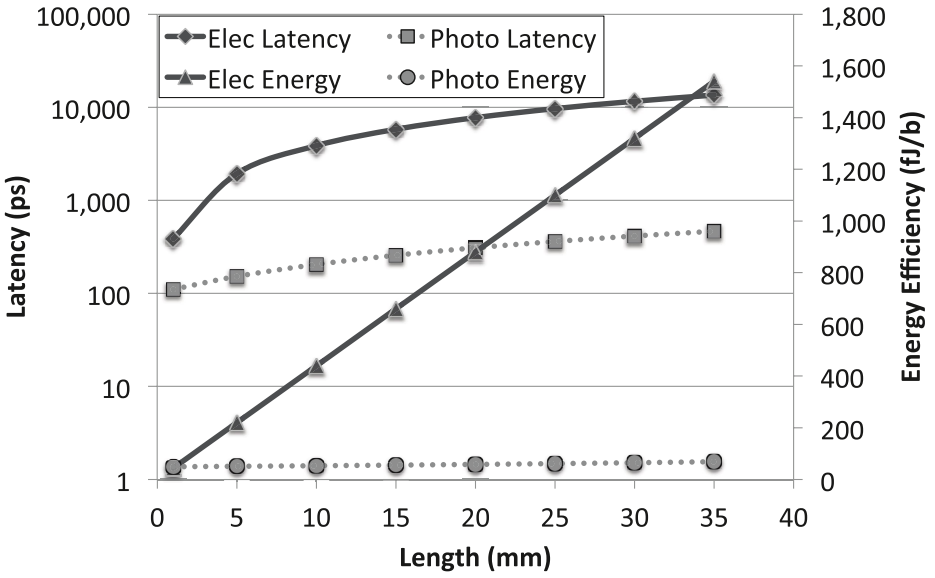


FIGURE 1.1: Latency and energy efficiency of electrical and optical interconnects as a function of distance for a 16nm technology (source ITRS)

The major advantages of Optical Interconnects (OI), compared to electrical interconnects in terms of latency and energy efficiency, appear for long distances between source and destination nodes. Furthermore, two important advantages must be considered. Firstly, the increasing data rate will not change energy efficiency because the optical loss does not depend on the data rate. Secondly, optical interconnects can increase bandwidth and data rate by using wavelength multiplexing division (WDM) technology. WDM multiplexes multi-optical carrier signals into a single optical wave-guide by using different wavelengths. Finally, compared to electrical links, optical links can also provide many communication strategies: point to point, broadcast, and varying bandwidth.

There are many reasons to claim that OI can overcome the bottleneck of electrical interconnects based on the signal propagation principle. In the optical domain, the optical signal carries information at a very high frequency and this signal is carried within the optical wave-guide. Then the optical signal is crosstalk and reflection immune. These advantages ensure that optical link has significant ability to support communications not only for long distances but also for on-chip interconnect multiprocessor systems.

1.1.2 Three-Dimensional Integration

Future on-chip multi-core processor systems face a challenge due to the increasing amount of integrated IP cores on a single chip. These challenges are putting inflexible requirements for the MPSOC designer. Recently, optical interconnects show the possibility to become an emerging solution for on-chip interconnects due to their advantages of high bandwidth, high energy efficiency and low latency. Some of the approaches using ONoC have been recently proposed. These approaches are based on the integration of Optical NoC (ONoC) on a specific silicon wafer/layer. However, the disadvantages of this integration are the complexity and the optical wave-guide crossing losses. 3D-stacked technology is one of the promising solutions which can solve the communication problem between these layers. This technology allows for the integration of ONoC in multi-layer. This approach can reduce the wave-guide crossing, one of the main factor impacting the power budget of optical interconnects. Furthermore, 3D stacking provides a significant cost advantage, which leads to the simplification of designs as well as the manufacturing process.

As we can see in Figure 1.2, a 3D ONoC is composed of an optical layer located between several electrical layers. Each electrical layer contains the Electrical NoC (ENoC) which is used to route the control packets and configure the Optical Network, whereas the optical layer includes the ONoC which consists of optical components such as lasers[2] [119], modulators [7, 92], photo-detectors [44], wave-guides [7]. In order to transfer data among

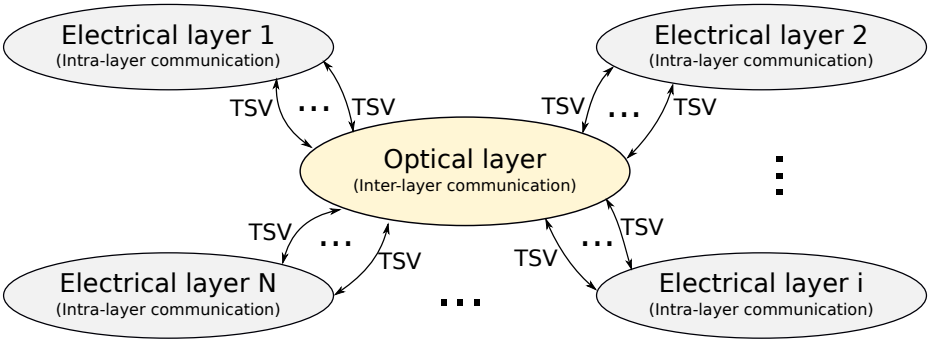


FIGURE 1.2: Architecture organization of a 3D Optical NoC [9]

electrical and optical layers, vertical interconnects through TSVs are employed. Communications between nodes of the different electrical layers (inter-layer communications) are supported by ONoC. Nodes on the same electrical layer communicate by intra-layer

[2]The term "lasers" originated as an acronym for "light amplification by stimulated emission of radiation."

communication. Recently, some companies have used 3D stacked technology in their chip manufacturing. For example, in 2007, IBM introduced chip with 3D-stacked technology [90]. In 2010, a new 3D-stacked technology which can integrate 100 silicon chips in a single package was proposed [91]. Even if 3D stacked technology can be interesting, it also induces new challenges, such as thermal problems. Indeed, thermal increase can lead to several undesirable effects such as the increase in power consumption, performance degradation and it generally reduces the reliability of the overall system. Recently, several approaches have been proposed for thermal issue management, for example by addressing new network topologies or task mapping.

To conclude, 3D ONoC is one of the most promising technologies for the next generation of MPSoC interconnects since it has the potential to reduce the interconnect length and the power consumption. However, 3D ONoC still has many open problems such as the design of optical network interface.

1.2 Thesis Contributions

3D ONoC is a potential candidate in future MPSoC architecture. In this type of architecture, the electrical layers are connected to the ONoC by using vertical interconnects (TSVs) to upload and download the data between the different layers. More precisely, to emit optical data, the TSV is directly connected to an optical modulator to drive an on-chip laser source which is located in the transmitter of the optical network interface (ONI). At the receiver part of the destination ONI, a TSV is connected to a pair of micro-resonator and photo-detector. The transmission will be performed in a serial manner in order to reduce the number of TSVs. According to the capacity of optical interconnects with high throughput, the data serialization requires a high-performance ONI which has to be designed to modulate and demodulate data emitted between electrical and optical domains. Modulation and demodulation need to be performed at high frequency to provide high bandwidth.

To address the Optical Network integration challenges, we propose a set of contributions which are summarised in the Figure 1.3. This figure illustrates the contributions of the thesis according to three main problems.

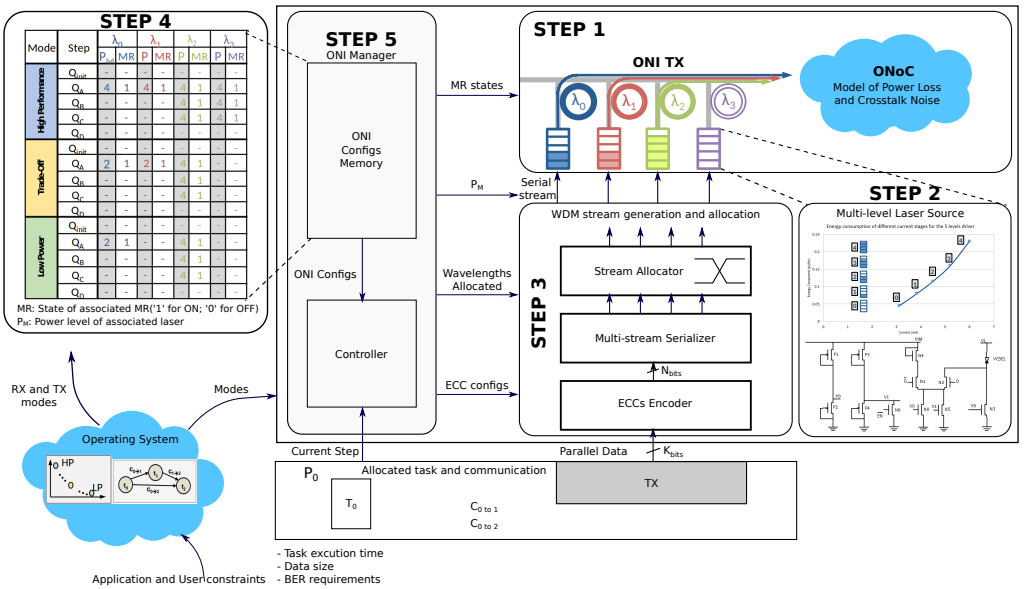


FIGURE 1.3: Representation of the components required for ONoC and highlight of the thesis contributions

- **Energy efficiency on-chip optical interconnects based on the state of the art of Error Correcting Codes (ECC)** (Step 1 and Step 3): ECCs have proved their abaility in optical communications [72, 100] or wireless sensor networks (WSN). From this context, we take advantage of ECC to improve the energy efficiency of optical interconnects for MPSoC. Our approach demonstrates the improvement of optical interconnects in terms of energy efficiency and communication reliability. The aim of this contribution is to find a trade-off between energy and performance.

- **Design of high-performance optical interface based on the ECC** (Step 2 and Step 4): The design of the ONI is one of the most important factors that contribute to the overall system performance. To the best of our knowledge, there are no global solution in the state of the art. Therefore, in this thesis, we propose the first complete optical network interface for WDM ONoC. This interface allows bandwidth and latency adaptations according to the different communication strategies.

- **Management unit for the optical network interface** (Step 4 and Step 5): Based on the interface architecture and the design of the laser driver, we propose a management unit for the optical network interface. This ONI manager consists of an ONI configuration memory, which receives data from allocation protocol, and

a controller which is driven by allocated tasks and operating system. We have designed this interface, and evaluations and synthesis results of this unit are provided.

1.3 Dissertation Organization

The thesis dissertation is organized as follows. In Chapter 2 , we present the state of the art in which the detail of optical devices and structure of optical link are firstly described. Secondly, our target architecture and Optical Network Interface are presented. Thirdly, state of the art in terms of Error Correcting Code (ECC) with related works in optical communication and WSN are presented. In Chapter 3, we model and analyze the optical losses and the crosstalk in WDM communications. We define the mathematical formulations of the different losses and we also propose a global mathematical model for a point to point communication. In Chapter 4, we propose an energy efficient optical interconnect based on ECC. In this chapter, we propose to use ECCs to improve the energy efficiency in order to meet the communication requirements. Since we model the structure and losses of optical interconnects, we establish the trade-off between energy-efficiency and system performance. In Chapter 5, we propose the complete design of the optical network interface in which the ONI has to be implemented as a co-design of both electronics and photonics domains, and where network issues, such as flow control, serialization, deserialization, and ECC integration, must be carefully evaluated. Furthermore, in this chapter, we also present the design of a management unit located in the electrical layer to control the interface and optimize the number of allocated wavelength according to the application requirements. Finally, conclusions and issues for future researches are discussed in Chapter 6.

Chapter 2

State-of-the-Art

Currently, optical interconnect is an attractive solution to address scalability issues in on-chip communication with low-power consumption, low latency, and high data rate and bandwidth. Some techniques, like error-correcting codes (ECC) have been used to improve the communication quality. In this chapter, an overview of optical interconnects including optical devices, like microring resonator, waveguide, photo-detector, and laser, is firstly presented in Section 2.1. Secondly, the classification of optical interconnects is described in Section 2.2 and several optical network-on-chip architectures are also presented. Thirdly, the main principle of ECC is presented in Section 2.4 and the use of this technique for ONoC is introduced. Finally, Section 2.5 concludes this state-of-the-art chapter.

2.1 Photonics Interconnect

Compared to electrical interconnects, on-chip optical devices show a great potential to become an emerging candidate for on-chip interconnect due to their properties (low latency, high bandwidth, and low power consumption). In this section, we present an overview of the candidate optical interconnect of Figure 2.1 that directly connects a source and a destination. It is composed of three main parts: a transmitter, a receiver, and a medium. In Figure 2.1, the laser is an off-chip laser which can emit multiple wavelengths for the communication. These wavelengths are injected into the waveguide and they are modulated by the microring resonators (MRs). The transmitter consists

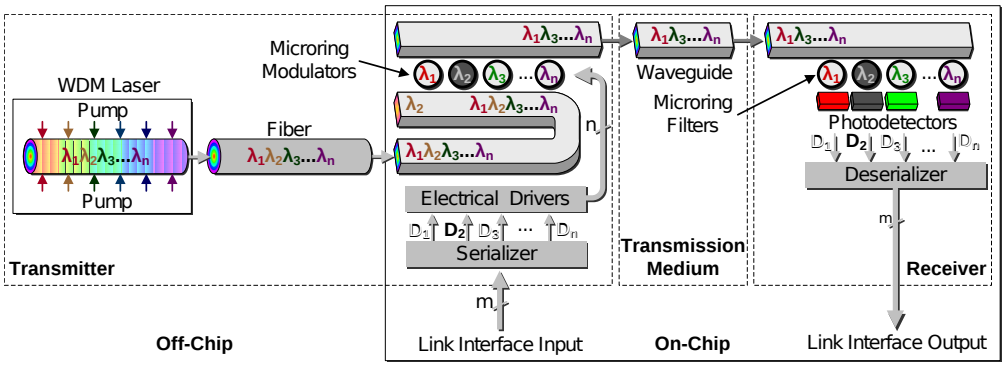


FIGURE 2.1: Overview of an optical interconnect using off-chip laser [74]

of the combination of the external laser, waveguides, serializer, electrical drivers and microring resonators. The signal is driven on the medium (waveguide) until it reaches a resonator which extracts and drives it towards the photodetector. At the receiver side, the signal is converted from the optical domain to the electrical domain by the photodetector and the serial data are converted into parallel data. Finally, the signal is transmitted to the destination by an electrical network which is located in the electrical layer.

2.1.1 Transmitter

The transmitter converts the electrical signal into the optical signal. An optical transmitter includes a laser, a driver network, and a micro-ring resonator. In the following sections, the main optical devices are introduced step by step.

2.1.1.1 Lasers

The position of the laser source can be categorized into two main types: on-chip and off-chip lasers. **In this thesis, we focus on on-chip laser integrated into the same die with the other parts of the interconnect**, without using an optical coupler to bring the light into the chip. We consider both modulation schemes: indirect and direct modulation. Compared to the off-chip laser, the on-chip laser can provide three key following advantages:

- First, it simplifies the integration in the design by relaxing constraints on the layout. Furthermore, the additional cost from an external laser source to the on-chip modulator is removed.

- Second, the flexibility and scalability of the network can be improved by optimizing the laser source placement on the layout.

- Third, the power consumption reduction can be enhanced by run-time management which can turn-on the laser when the communication occurs or turn-off when there is no communication to ensure. Furthermore, on-chip lasers with low-power consumption can be obtained by reduction of loss due to communication crosstalks. Moreover, for off-chip laser, the loss path is not only from source IP to destination IP, but also from the off-chip laser to source IP. Therefore, by using the on-chip laser, we can reduce the global loss and then reduce the required laser output power.

On-chip light source is an imperative and important device of silicon photonics technology. With features advantages, the on-chip laser shows the potential to become the enabling technology of on-chip light source. Recently, some new technologies have been presented for on-chip laser like Fabry-perot (FR), Distributed Feed-back (DBR) and Micro-disk [12, 80, 22, 101, 21].

Vertical cavity surface emitting laser (VCSELs) is also an interesting technology due to the footprint size as well as straightforward fabrication [5]. Particularly, VCSEL can provide the output power in the range of hundred microwatts, which can adapt the requirement of current and future nanophotonic interconnect. Additionally, double photonics crystal mirror VCSEL (PCM VCSEL) based on a complementary metal-oxide semiconductor are CMOS compatible, which allows for DWDM direct modulation and indirect modulation [94]. Thus, VCSELs are sufficiently compact to implement a large number in a single chip. By specializing the topology, we can avoid the waveguide crossing losses, which is a very costly element contributing to the power budget of the overall system.

As previously mentioned, the main role of the laser is to produce the optical signal that will be sent into the waveguide. But this optical signal must also transport the information (data) from sender to receiver and, to ensure this feature, the optical signal must be modulated. There are two methods to modulate the signal: direct modulation (internal) and indirect modulation (external). The direct modulation method is the technique for which the optical signal is directly modulated by turning on or off the laser source (Figure 2.2.a). In the indirect method, the optical signal is always on. Meanwhile, the light

is modulated by an external device (MRs modulator) in order to control the light flow through the optical waveguide as illustrated in Figure 2.2.b.

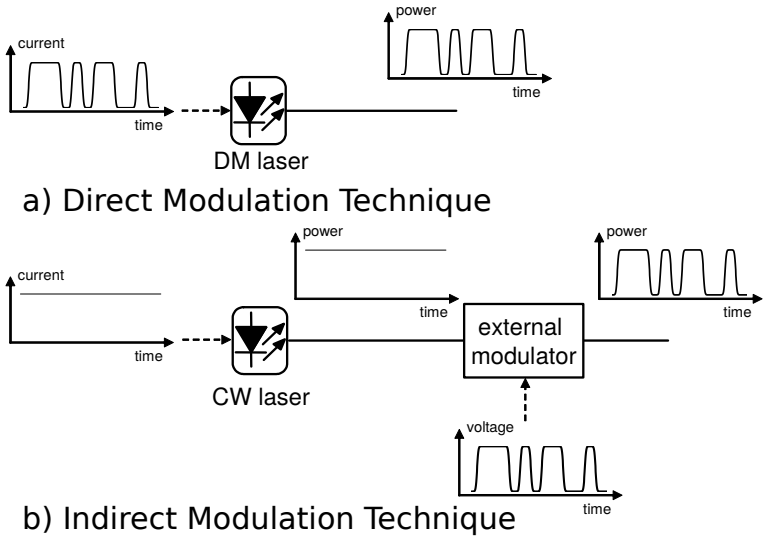


FIGURE 2.2: Modulation schemes: a) direct modulation technique and b) indirect modulation technique [81]

2.1.1.2 Microring Resonators

A Microring Resonator (MR) is an optical device which is built for optical interconnects. The main role of MR consists in extracting a specific wavelength from an optical signal and injecting this wavelength to another waveguide. The resonance of the wavelength can be modified to control the extraction or injection of the optical signal into the waveguide. Figure 2.3 illustrates the structure of an MR with a diameter of $12\mu m$. This is a passive

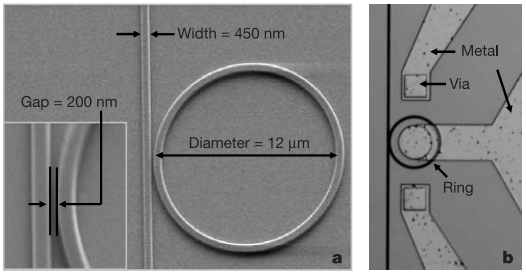


FIGURE 2.3: Structure of an actual $12\mu m$-diameter passive microring

MR used for moving a certain wavelength from the waveguide to another. Figure 2.4.a and Figure 2.4.b show a microring Resonator in the OFF-resonate state and ON-resonate state, respectively. Each MR can be resonated at a given wavelength. When the MR is in OFF state, the wavelength continues in the main waveguide (from input to through

ports). Whereas, when the MR is turned ON, the wavelength is extracted from the main waveguide and injected inyo the second waveguide (from input to drop ports).

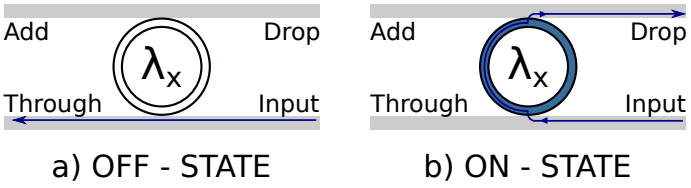


FIGURE 2.4: Microring Resonators states a) Off state; b) On state.

The resonated wavelength depends on both MR's diameter and effective refractive index [7]. These parameters are affected by the electrical charge and the thermal issue.

Based on the fabricated method, there are two types of MR: passive MR and active MR. The active micro-ring is used as a modulator to modulate the light which is emitted from the laser source (see Section 2.1.1.3). The active MR is used as an optical switch. It is biased during fabrication to extract only a single wavelength from one waveguide and reflect the others. The function of MR is similar to a switch with two states: OFF-resonate and ON-resonate. The wavelength is selected to drop into the MR. Furthermore, in order to avoid the optical crossing loss, which is one of the major factors impacting the energy efficiency, the MRs can be configured in parallel or perpendicular waveguide configuration. Figure 2.5.a and Figure 2.4.b show the MR in ON-state and OFF-state with λ_1 in

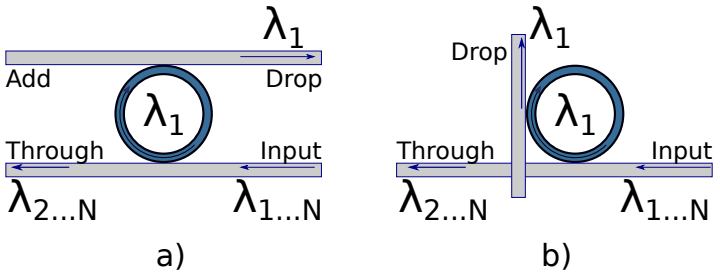


FIGURE 2.5: Waveguides and MR positions; a) parallel configuration; b) perpendicular configuration

perpendicular and parallel waveguides configurations, respectively. In the perpendicular waveguide configuration, multi-layer technology are used to avoid the waveguide crossing losses (0.05dB to 0.2dB [10]). Communication between layers can be implemented by using vertical grating couplers as we can see in Figure 2.6.a. The perpendicular waveguide configuration is shown in Figure 2.6.b using vertical grating couplers. Due to its simple response, MRs can be used to build many important optical components such as optical router, optical switch, optical modulator and detector. However, MR is a device that is

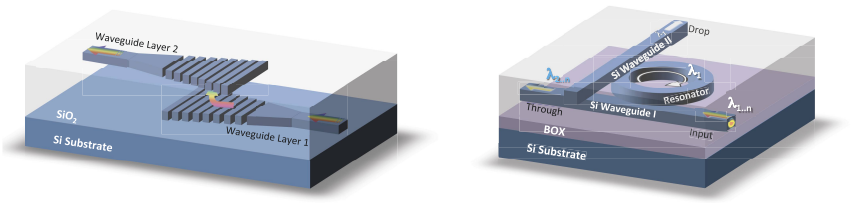


FIGURE 2.6: a) The MR in parallel configuration is turned ON to select λ_1 wavelength; b) The MR in perpendicular configuration is turned ON to select λ_1.

very sensitive to temperature issues. Therefore it can become a major source of errors if the temperature is not stable. In particular, MRs can suffer from the important shift in its resonant wavelength due to temperature increase, which can lead to stopping extraction from a waveguide or injection to a waveguide. Thus, architecture considerations need to be explored in order to improve interconnect energy efficiency.

2.1.1.3 Modulators

As explained before, the modulation can be direct or indirect. When the modulation is direct, the photonics device which supports this feature is the laser. But when the modulation is indirect, the photonics device which supports this functionality is generally a microring. Indeed, because the resonance frequency of MR can be changed (by the carrier depletion), it can be used as a modulator. In this case, the MR is an active component which is controlled to modulate the optical signal from data to transport.

In the context of optical interconnects, on-off keying (OOK) coding is the simplest modulation technique which can adapt the communication speed and bandwidth requirements due to its simple implementation. In this method, logic '1' is represented by the presence of light in a given wavelength and logic '0' is the absence of light in this wavelength. This coding can be created by controlling an active MR (see Section 2.1.1.2) to:

- extract a wavelength from a waveguide and drop it onto another waveguide (case of '1'),
- let the wavelength pass through the MR without extraction (case of '0').

In order to control the MR, an electrical current is used to change the refractive index by changing the bias voltage applied on the modulator. Figure 2.7 shows the layout and DC measurement of an MR modulator in which the inset shows the cross-section of

the microring. R is the radius of microring resonator. V_F is voltage applied on the MR modulator.

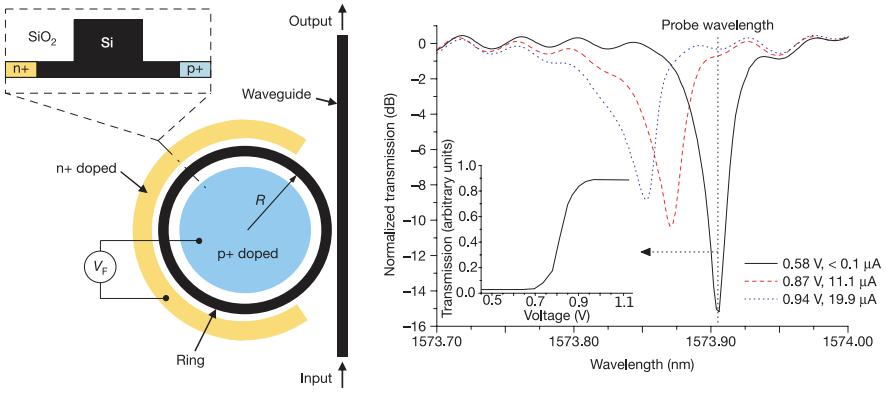


FIGURE 2.7: a) Layout of the ring resonator-based modulator b) Transmission spectra of the ring resonator at the bias voltages of 0.58 V, 0.87 V, and 0.94 V, respectively.

2.1.2 Optical Medium

Optical medium is the key component to transfer the optical signal between the transmitters and receivers in 3D ONoC. Based on the material, we can classify into different kinds of media: Air, SiO_2, Si_3N_4, etc. In this section, we present some transmission media with different configurations and materials.

2.1.2.1 Waveguide

As depicted in Figure 2.8, there are four main configurations of waveguides: channel, ridge, slot, and photonics-crystal. Among them, the channel and ridge (Figure 2.8.a and Figure 2.8.b) are the most popular configurations used in on-chip interconnects [50]. Slot and photonics-crystal configurations (Figure 2.8.c and Figure 2.8.d) are less common.

Figure 2.9 shows the cross-sectional structure of a waveguide which consists of different refractive indexes: a core with high refractive index surrounded by a lower refractive index material which is called cladding material. In the context of on-chip interconnects, there are many materials to construct the optical waveguides such as: glass, polymer, or semiconductor. Among them, semiconductors show the potential to become an emerging material due to their characteristics which can make a very high contrast between core and cladding. Especially, Silicon has shown its ability to become an attractive candidate

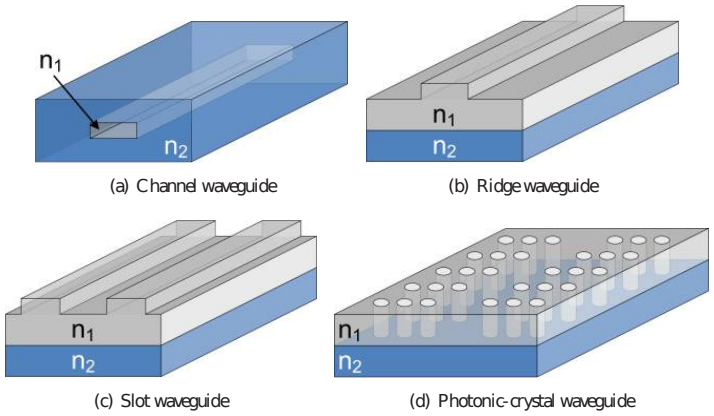


FIGURE 2.8: a) Channel b) Ridge c) Slot and d) Photonic-crystal waveguide configurations.

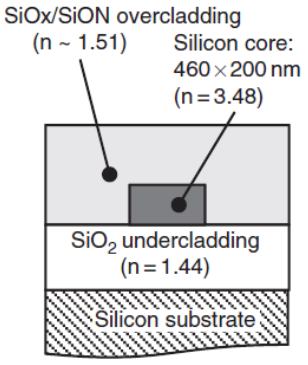


FIGURE 2.9: Cross-sectional structure of a typical cladding waveguide.

due to CMOS compatibility in the fabrication. Therefore, **in this thesis, we assume that the material to construct waveguide is Silicon**, although it could be glass, polymer or another semiconductor materials.

In addition, insertion optical loss is an important factor which affects the overall power consumption of the optical interconnect. Therefore, the loss of waveguide must be analyzed to explore carefully the optical network-on-chip architecture trade-off. In the optical waveguide, optical losses are composed of material absorption, scattering and two-photon absorption (TPA) [95]. Furthermore, the bending loss and waveguide crossing loss are the other sources of loss [40, 78, 47]. According to [59], the absorption of light in silica and silica oxide is negligible compared to the others. However, the crossing loss is the most important factor which directly impacts the power consumption in ONoC due to its high effect on communication quality. Therefore, in order to avoid the waveguide crossing and improve the power efficiency, the multi-layer technology could be used to replace single layer as illustrated in Figure 2.10. Waveguide crossing can be avoided by using multi

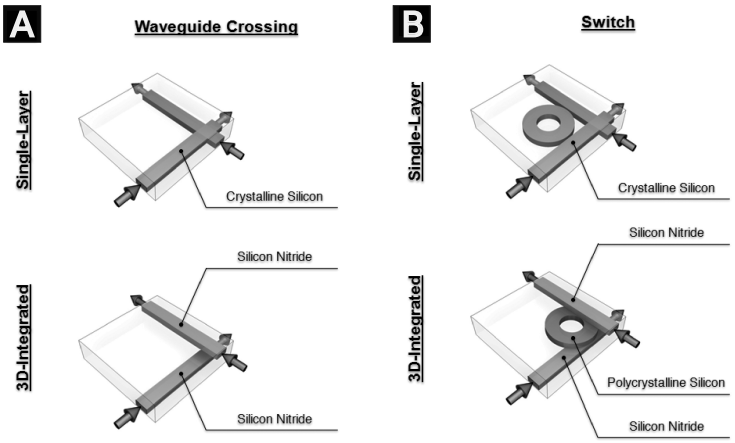


FIGURE 2.10: Waveguide crossing and Switching Element for both single-layer and 3D-integrated approaches [10]

optical layers technology. Indeed, the waveguide crossing (Figure 2.10.a) and switcher (Figure 2.10.b) are the most popular components used in optical network on-chip. The potential of the multi-layer technology can eliminate the waveguide crossings created by these elements, and improve the energy-efficient of optical interconnect.

2.1.2.2 Through Silicon Via

In the 3D integrated circuit paradigm, Through Silicon Via (TSV) [39, 69, 110] is used for data transfer between different layers. Figure 2.11 illustrates the position of TSV in the interface of a potential 3D ONoC. An uploading TSV is used for connecting the

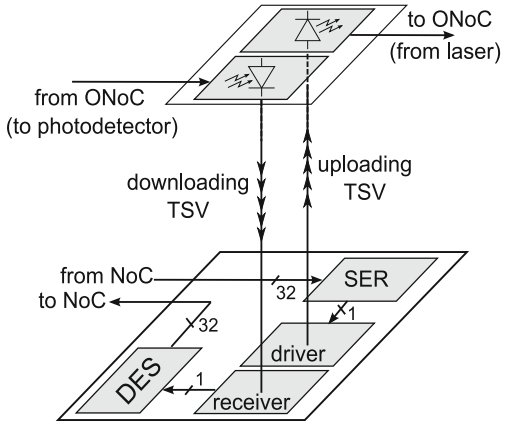


FIGURE 2.11: TSV's position in the optical network interface in the context of 3D ONoC [54]

electrical layer with the optical layer, then the electrical signal is used to modulate the

optical signal. A downloading TSV is used for connecting the optical layer to the electrical layer. At the optical layer, a photo-detector is used to convert the optical signal into the electrical signal, which is then transported by TSV. Size and pitch of TSVs are very important factors which impact the overall footprint. It is then clear that a trade-off must be found between the area needed for an Optical Network Interface (ONI) and the area of a set of processor cores, grouped in a cluster, which is connected to this ONI. Figure 2.12 shows the TSV size evolution according to ITRS. In this figure, the

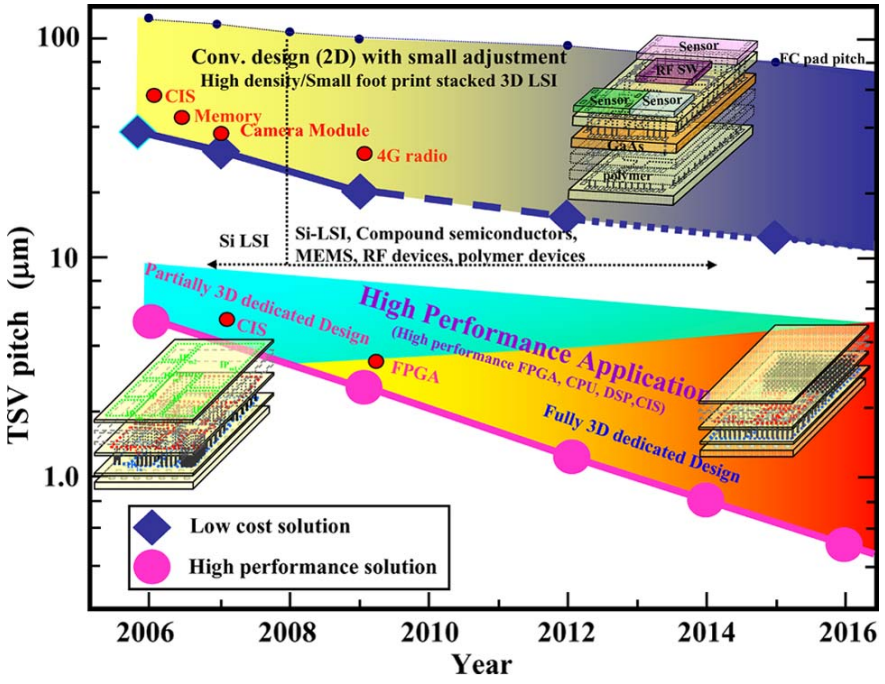


FIGURE 2.12: TSV for three-dimensional large-scale integration (3D-LSI) technology roadmap from [69]

current TSV technologies for 3D-LSI are classified into two types, according to their sizes, and it appears that TSVs can become a dominating technology in the future of three-dimensional large-scale integration. In particular, TSV reduces the length of interconnects as well as the size and pitch of interconnects compared with the other interconnect technologies. Although TSVs provide many advantages such as electrical performance, low-power consumption and higher data bandwidth, it also presents some drawbacks which lead to some design challenges such as testing process, power distribution and thermal issue.

Therefore, the need for design exploration is very necessary to evaluate the interest of this technology.

2.1.3 Receiver

Optical receivers must support several functions which are: i) receiving optical signals, ii) converting them into electrical analog signals, iii) processing and restoring digital signals. In this section, we will present the general structure of an optical receiver in the context of on-chip optical interconnect. As the main part of the receiver is composed of photo-detectors which convert signals from optical to electrical domains, a classification of photo-detectors and the sensitivity of optical receivers are also presented.

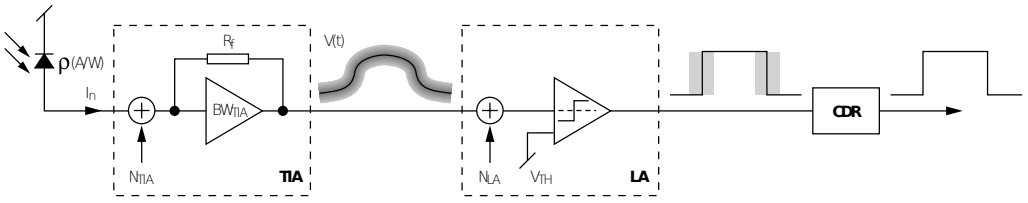


FIGURE 2.13: Structure of a single-wave optical receiver.

The structure of a typical optical receiver is illustrated in Figure 2.13. It consists of a photo-detector (PD), a trans-impedance amplifier (TIA), a limiting amplifier (LA), and a clock data recovery (CDR) block. For the case of WDM scheme communications, each PD is associated to an MR to extract the corresponding optical signal from the main waveguide [14].

In Figure 2.13, the optical signal is directly extracted from the optical waveguide and sent to the photo-detector. The photo-detector converts optical signals into electrical currents. This current is transformed into a voltage which is then amplified by the trans-impedance amplifier. The limiting amplifier acts as a comparator with a threshold voltage V_{th}. Clock-data recovery will then restore the original signal.

As one of elements of the optical receiver, PD is an optical device that directly converts optical signals into electrical signals. Currently, there are many types of photo-detectors used in Optical Network on-Chip with a variety of materials and structures such as silicon photo-detector [13], III-V semiconductors [38] and Germanium photo-detector [102].

Based on their structure, we can classify photo-detectors in two types: P-I-N photo-diode (PIN) [29] and avalanche photo-diode (ADP) [37]. In the context of on-chip optical interconnects, PIN photo-detector has been widely used as the optical receiver [29],

[44] due its its advantages in terms of dark current, responsivity, operation speed, and footprint.

To obtain the power budget of the optical link, one important factor that needs to be considered is the photo-detector sensitivity. The sensitivity (in dBm) is the minimum optical power required at the receiver to achieve a given BER value. For example, if a sensitivity is $P_{sen} = -25dBm$ at $BER = 10^{-9}$, this means that if the optical power at the optical receiver is greater than or equal to $-25dBm$, the system can operate reliably with $BER = 10^{-9}$. The computing of sensitivity and power budget will be presented in Section 4.4.3 in more details.

2.2 Optical Network on-Chip – Some Case Studies

Recently, many WDM-based ONoCs have been presented in the literature with different designs. The differences between these designs come from their architectures and the components used to build the communication infrastructure.

More generally, ONoCs can be classified into two main categories: i) Circuit Switching ONoC and ii) ONoC based on Optical Crossbar. They will be described in more details in the following sections.

2.2.1 ONoC based on Circuit Switching

As mentioned in Section 2.1.1.2, an active MR is a micro-ring which can be used as an optical switch to transmit the light in an optical waveguide. Hence most of the optical switching circuit interconnects are implemented based on active MR components. This kind of MR requires an electrical control network to change the state of the wavelength resonance by changing the reflective index. In circuit switching interconnects, the data transmission is divided into three steps. Firstly, control packets are routed in the electrical control network in order to reserve the optical path and configure the active micro-rings. Secondly, when the control packets are completely sent from the source to the destination, the optical path is established and active MRs are configured to turn ON or turn OFF based on traffic requirements. The optical data are sent directly from source to the destination. Finally, once the optical transmission is completed, an erase packet is sent

to relax the communication path and the optical devices. This transmission of erasing packet can also be used to prepare the reservation for the next communication slot.

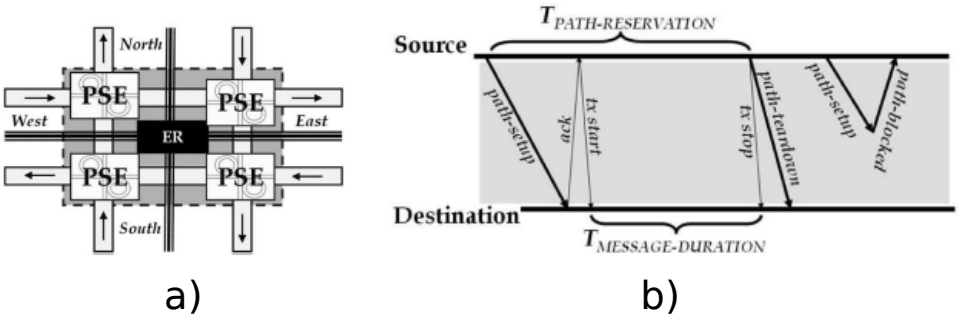


FIGURE 2.14: a) Basic optical router based on MRs, b) Qualitative timing diagram of a successful optical path setup and a blocked setup request [97]

Figure 2.14.a and Figure 2.14.b show the structure of router based on the Switching Circuit and the setup process in optical switching circuit interconnects [97]. Figure 2.14.a presents an optical router structure based on the four PSE (photonic switching elements) controlled by an electronic router (ER). In Figure 2.14.b, the timing diagram illustrates the timing discrepancy which includes the time to reserve the path before sending the packet to the destination. The disadvantage of an ONoC based on switching circuits is the time to set up the optical path which can reduce the latency and increase system power consumption. Recently, several ONoC based on switching circuits have been presented. For instance, [32, 109, 117] present ONoCs with Mesh topology, [118, 96] with Folder Torus, and [33] with Fat-Tree topology. All of them suffer from reservation time in the optical path which can be long.

Therefore, switching circuit technique can become a major challenge of the ONoC design. This problem can be solved by using the ONoC based crossbar introduced in the next section.

2.2.2 ONoC based on Optical Crossbar

Crossbar ONoC is based on passive MRs which are set up to select a given wavelength. Therefore a source IP can directly send the data through the optical router with one or several predefined wavelengths. In crossbar ONoC, due to the property of passive microring which does not need to be tuned (MRs are already set up before the communication occurs), the message transmission does not require the time to set up the optical path

and the time to relax the MRs after finishing the transmission. Compared to switching ONoC, this technique has the advantage to reduce the overall latency. However, conflicts can appear in optical routers of the crossbar ONoC when many communications occur at the same time. These conflicts can be solved by using an arbitration that can be implemented by an optical network or an electrical network. For instance, when a communication occurs between a source and a destination at a given time, the destination cannot receive any data from other sources. Then, the destination sends a message to the arbitration to decline other connected requirements from other sources. The potential of the arbitration compared to the electrical control network of switching circuit network is the latency.

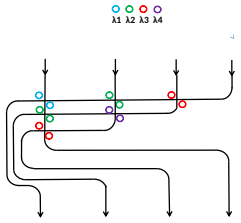
Because passive MR does not require the time for reservation as well as the time to relax after finishing the communication, this technique can exploit all the properties of the optical network which are the high bandwidth and the low latency. Furthermore, the power consumption of passive MRs is less than the power consumption of active MRs which require a bias current to be controlled. Then the power consumption of the overall system can be reduced. **In this thesis, we focus on crossbar ONoCs** with four different communication schemes. The following section introduces some of the existing ONoCs based on optical crossbars.

2.3 Survey of Existing ONoC Architectures Based on Communication Schemes

This section describes some case studies of the optical crossbar based interconnects with different architectures. Based on the communication schemes, there are many optical interconnects with different structures: SWSR (Single Writer Single Reader), MWSR (Multiple Writers Single Reader), SWMR (Single Writer Multiple Readers), and MWMR (Multiple Writers Multiple Readers). In this section, we present step by step these different structures. Each structure is illustrated by a typical example with its corresponding features.

2.3.1 Single Writer Single Reader

SWSR is the simplest interconnect scheme. It relies on the wavelength routing between a source and a destination IP. For instance, Figure 2.15 illustrates the architecture and the connectivity strategy of the SNAKE ONoC [88]. SNAKE is a wavelength routing archi-



	T1	T2	T3	T4
I1	λ_1	λ_2	λ_3	λ_4
I2	λ_2	λ_4	λ_1	λ_3
I3	λ_3	λ_1	λ_4	λ_2
I4	λ_4	λ_3	λ_2	λ_1

a) b)

FIGURE 2.15: SNAKE ONoC a) architecture and b) connectivity strategy [88]

tecture based on passive MRs in which each pair of source and destination elements are connected by different wavelengths (Figure 2.15.b). The advantage of this communication scheme is its simplicity and low latency due to the non-blocking property. However, the disadvantage of SWSR is the lack of scalability which is limited by the number of optical resources such as the number of MRs, the number of wavelengths in a waveguide, and the number of lasers.

Another example of SWSR is the λ-Router represented in Figure 2.16 [11]. This ONoC is a

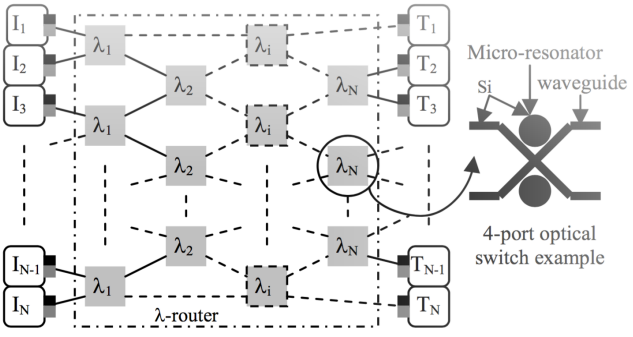


FIGURE 2.16: λ-Router a) architecture and b) connectivity matrix [11].

contention-free network, meaning that the λ-Router ONoC does not need any arbitration network. This property can be ensured because all destinations can receive the data without any conflict.

In ORNoC [53], Le Beux *et al.* present a new communication scheme for which SWSR channels can be reused by reusing the same wavelengths for different communications in

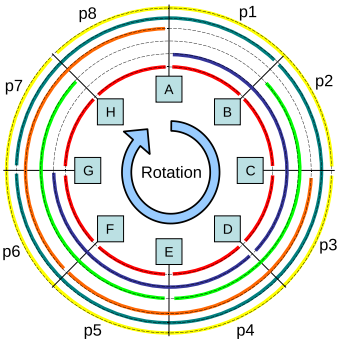


FIGURE 2.17: Optical Ring Network On-Chip (ORNoC) [53]

different parts of the waveguide. This technique is really interesting in particular because it can improve the energy efficiency. Figure 2.17 illustrates the architecture of ORNoC. In this architecture, the IPs are connected by ring topology waveguides. In the example presented in this figure, the waveguide supports 6 wavelengths which can be used together as communication channels to improve the bandwidth. As we can see, the red wavelength can be reused to connect the IPs from A to H. In order to improve the scalability and bandwidth as well as the energy efficiency, the SWSR can be extended to MWSR as presented in the following section.

2.3.2 Multiple Writers Single Reader

In MWSR, each IP source (processor core or cluster of cores) can send the data to all the remaining IPs but can only receive the data from one of them. This scheme of communication is illustrated in Figure 2.18 where an MWSR with four nodes is presented. In this example, Node 2 transmits data to Node 4. In this architecture, all of the three

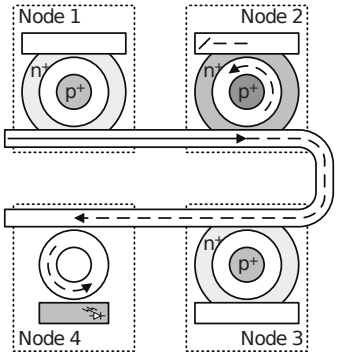


FIGURE 2.18: A four-cluster single-bit MWSR bus

clusters (Nodes 1, 2, 3) can transmit to the remaining cluster (Node 4) using the same waveguide with different wavelengths.

A typical example of this kind of communication scheme is CORONA [105]. Figure 2.19

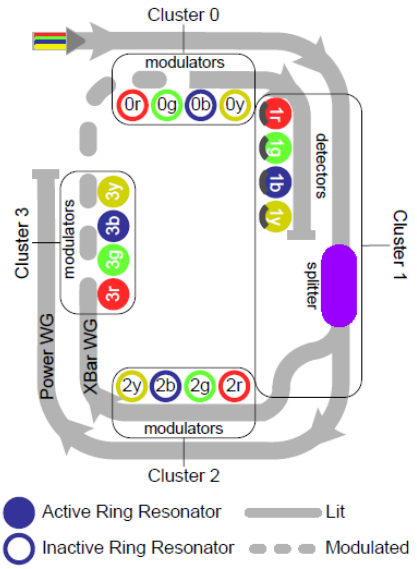


FIGURE 2.19: A Four Wavelength Data Channel Example of CORONA [105].

illustrates the architecture of CORONA in which MWSR is implemented. CORONA uses a 256-bit optical crossbar operating at 10 GHz to ensure communication between 64 clusters (each composed of four processor cores). CORONA combines arbitration and control flow into a single flow called optical token-based.

2.3.3 Single Writer Multiple Readers

SWMR (also called "broadcast" communication scheme) is implemented by allowing the communication between one source IP and all remaining destination IPs [79, 48]. Figure 2.20 illustrates the SWMR communication scheme with the Firefly architecture. The source router R_0 broadcasts data to all the other $(N-1)$ routers. To ensure this communication, all the receivers must extract part of the optical energy from the waveguide, and all the photo-detectors must be aligned to the wavelength used by the sender. Therefore the laser power at the source side must be high enough to ensure that all receivers obtain sufficient optical power. In this case, more than $N-1$ times of the normal power must be produced by the sender to ensure detection on each receiver. In this communication scheme, by default, all the destinations are turned off. In step 1, by sending a reservation flit which contains the receiver address information and packet length (Figure 2.20.d), the corresponding receiver is turned ON to receive the data in step 2, while the others are turned OFF. Then, the power consumption needed for broadcast can be saved.

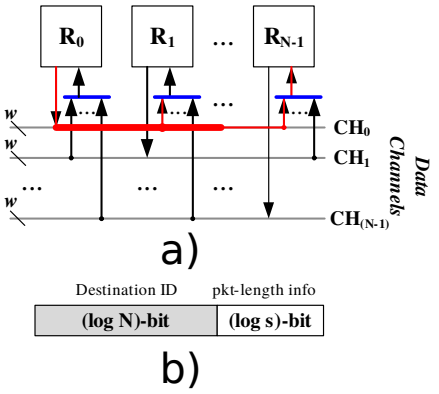


FIGURE 2.20: Implementations of the Firefly nanophotonic crossbar (a) Single-write-multi-read bus (SWMR), (b) Reservation flit [79].

2.3.4 Multiple Writers Multiple Readers

In MWMR, the combination of SWMR and MWSR is implemented in order to allow for all the source and destination IPs to access the interconnect medium. Compared to SWMR and MWSR, this communication scheme leads to the increase of optical insertion loss which is the main reason of high power consumption. Figure 2.21 illustrates the

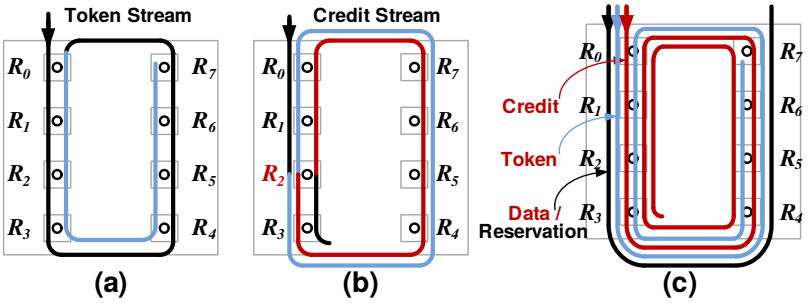


FIGURE 2.21: (a) Token stream waveguide, (b) Credit stream waveguide, (c) Waveguides for all the three types of channels [78].

Flexishare architecture which uses a token-stream based arbitration network to assign the wavelengths. Figure 2.21.a shows the waveguide for the token streams which passes each router twice. Figure 2.21.b presents the credit streams in which the laser must be routed to the router distributing the credits first and then traverse all the routers twice, as highlighted with different colors.

2.4 Error Correction Codes to Improve Energy Efficiency

In this thesis, we present some methods that use error correction codes to improve energy efficiency and reliability of optical interconnects. Considering the power consumption of

optical devices, the implementation of ECC in a global communication path can be very interesting. In this section, we present the basic concept of ECC and the state of the art of this technique from different perspectives: Wireless Sensor Networks, Optical Communications, and On-Chip Optical Interconnect, respectively.

2.4.1 Basic Concepts

Reliability and energy efficiency are the most important factors in digital communications. In such systems (digital communications, storage systems, etc.), error control is one of the most important techniques which contribute to the reliability and energy efficiency of the links. Hence, the use of error correction codes has become a critical problem in the design of such systems.

The basic concepts of ECC rely on the principle that some redundancy is added to the data to correct the errors which occur during the transmission. Figure 2.22.a shows

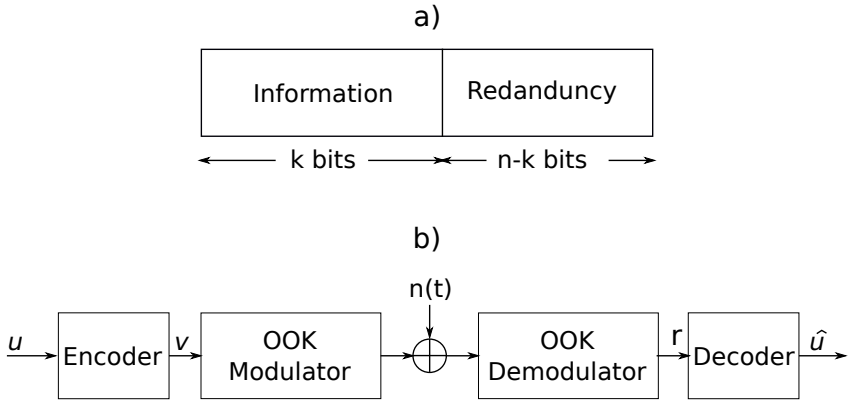


FIGURE 2.22: a) Concept of redundancy codes b) Example of a digital communication scheme [58]

the concept of block codes (systematic code[1] [58]) in which the right side (redundancy bits) is a function of the left side (information bits). Figure 2.22.b illustrates a coded digital communication in which a source sends the information bits (u), the encoder adds redundancy bits into the information bits. The data output of the encoder is called codeword (v) which consists of the information and redundancy bits (e.g., parity bits). During transmission through the medium, if some errors occur (due to the transmission noise), the decoder recovers the received bit (r) into the estimated information bits ($\hat{u}$).

[1] In coding theory, a systematic code is any error-correcting code in which the input data is embedded in the encoded output.

2.4.2 ECC in Wireless Sensor Networks (WSN)

Recently, there were many researchers focusing on error correcting codes for WSN. ECC has a very important role in this domain due to the error correction probability and energy efficiency properties. Studies of [36] and [93] examine the use of ECC in WSN for a range of ECC types which consist of both convolution and block codes. In addition, these publications provide the generic equation for the critical distance at which the ECC becomes energy efficient. Also, the implementation of several ECC schemes has been presented in these studies. In [106], Vuran *et al.* present the analysis and a comprehensive comparison between FEC (Forward Error Correcting), automatic repeat request (ARQ) and hybrid ARQ scheme in WSN. Recent researches focusing on convolutional and block codes for WSN are also presented in [98, 8, 41, 93].

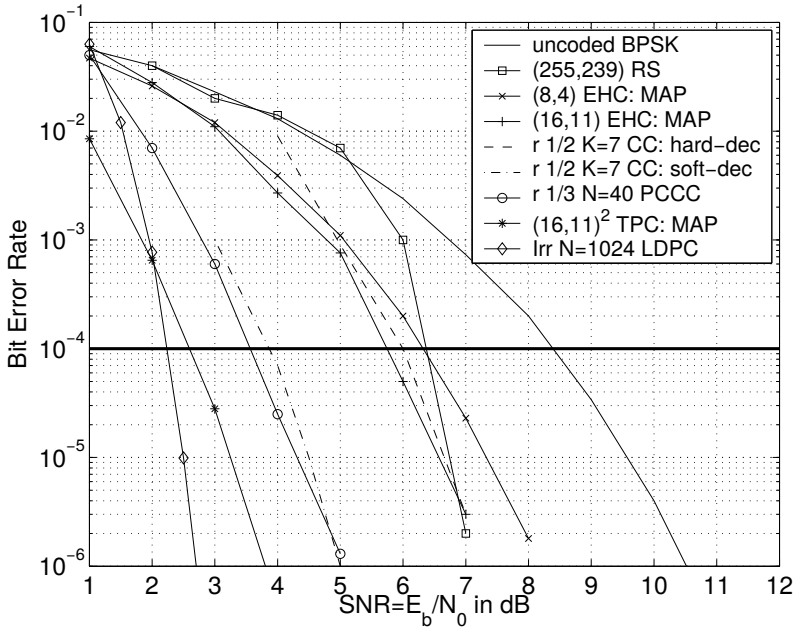


FIGURE 2.23: BER performance vs. SNR for several error-correcting codes [36].

Figure 2.23 compares the BER performance of some ECCs schemes [36]. As we can see in this figure, using ECC can provide significant lower SNR compared to an uncoded system.

2.4.3 ECC in Optical Communications

ECC is considered as a typical approach used to improve the reliability and to reduce the power consumption in optical communications. In long-distance optical communications,

the development of ECC can be divided into three generations which correspond to the increase of ECC coding gain. In early day, D.Grover presents FEC in dispersion limited light-wave system which provides 2.5dB at BER = 10^{-13} [31]. The first fully-fledged ECC for submarine optical transmission was deployed in the early 1990s. A typical example of the first generation is presented in [89] with Reed-Solomon codes RS(255,239). The second generation of FEC consists in the use of concatenated codes [30] for high-throughput DWDM submarine communications. The typical example of second generation FEC is $RS(239, 223) + RS(255, 239)$ [68]. The most powerful FEC is the third generation which are based on soft decision decoding technique [67]. A comparison between the three

TABLE 2.1: Summary of three generations of FEC (data extracted from [67]).

Gen.	Decision	Coding	Code rate	NCG(dB) @10^{-13}
1^{st}	Hard	Cyclic codes / Algebraic codes e.g. RS(255,239)	0.93	5.8
2^{nd}	Hard	Concatenated codes e.g. RS + BCH, RS + RS	0.93-0.79	<10
3^{rd}	Soft	Soft-decision & Iterative decoding e.g. Block turbo code, LDPC	>0.80	>10

generations of FECs is presented in Table 2.1 with the corresponding coding gain at $BER = 10^{-13}$

2.4.4 ECC for On-Chip Optical Interconnects

In optical interconnects (chip-to-chip interconnect or optical data link), ECC is also an approach to improve energy efficiency and reliability of communications links. In [75, 34, 70], the authors present the use of ECC based on ARQ to reduce the BER and optimize the bandwidth. In [34], the authors show the ability of FEC to relax the throughput and to improve the performance. The potential of FEC in two-dimensional optical data link with Golay codes to improve performance and reduce on-chip power consumption was demonstrated in [24]. For chip-to-chip optical interconnects, Jun Wang *et al.* present the comparison of different types of ECC using 90nm CMOS technology [107]. The experimental results presented in this paper conclude that ECC with Hamming code (87,80) is suitable for chip-to-chip optical interconnects. For on-chip interconnects, many methods of ECC using ARQ or Cyclic Redundancy Check (CRC) to provide a reliability optical link are presented in [73]. Also, Berger codes [6] are evaluated to detect

any number of unidirectional errors. However, Berger code implementations are too costly to become a good candidate for on-chip optical interconnects. In [26], a low complexity non-interactive BCH code[2] [15] is proposed to reduce the laser power and relax the stringent optical modulation amplitude requirements. This work is implemented using a 28 nm CMOS technology and results in 25% reduction of energy dissipation.

2.5 Conclusions and Thesis Contributions

In this chapter, we first presented the state of the art of optical interconnects with various optical devices in three main parts: transmitter, medium, and receiver. Then, some architectures of existing ONoCs were introduced. With low-power consumption, low bandwidth, and high bandwidth property, optical interconnects show the ability to become an emerging candidate for future of on-chip interconnects. However, in order to limit the effect of optical losses and crosstalk noise and to improve energy efficiency, we propose in this thesis the use of error correcting codes. ECC is not only used to improve performance but also to reduce power needed for the laser due to its error-correcting ability. Considering the solutions proposed in the state of the art, we address the three major following problems in this thesis.

Energy efficiency on-chip optical interconnects based on the state of the art of Error Correcting Codes (ECC). The advantages of optical interconnects rely on the optical devices properties which provide high bandwidth, low latency and low-power consumption. However, due to the optical loss and crosstalk noise which can lead to errors occurring during the transmission, these optical devices can reduce the performance of the system. In this thesis, we take advantages of the ECC to provide an energy efficiency optical interconnect for 3D MPSoC. Our approach demonstrates some improvements of optical interconnects in terms of energy efficiency as well as communication reliability.

Design of high performance optical interface based on ECC. In this thesis, we propose a complete optical network interface for coded optical WDM ONoC. This

[2]In channel coding theory, the BCH codes (Bose-Chaudhuri-Hocquenghem) form a class of cyclic error-correcting codes that are constructed using polynomials over a finite field (also called Galois field).

architecture of the interface leads to a simple design layout and allows for the adaptation of bandwidth and latency according to different communication strategies.

Optical network interface management unit. Based on the architecture of the optical network interface and the design of the laser driver which has been already addressed, we propose a management unit for the optical network interface. This ONI manager consists of several components, such as ONI configuration memory (which receives data from allocation protocol) and a controller (which is driven by allocated tasks and operating system).

In the next chapter, we model and analyze the optical loss and crosstalk noise which are two important factors contributing to the energy efficiency of the optical interconnect.

Chapter 3

Modeling and Analyzing Attenuation and Crosstalk in WDM ONoC

The attenuation and the crosstalk noise are very important factors contributing to the energy efficiency of the optical interconnect. The ONoC is constructed using MRs, which are one of the main sources of attenuation and crosstalk noise. In order to address the energy efficiency problem of optical interconnects, attenuation and crosstalk noise need to be explored and analyzed. This chapter is organized as follows. Section 3.1 introduces models of attenuation and crosstalk in ONoC. The architecture of CHAMELEON 3D ONoC is presented in Section 3.2. Section 3.3 details the fundamental analysis of attenuation and crosstalk noise at the device level. Based on this analytical model, Section 3.4 presents the analysis of crosstalk noise at the network level. Section 3.5 shows the results and discussion. Finally, Section 3.6 concludes this chapter.

3.1 Introduction

The technology scaling down shows the potential of optical interconnects to replace the electrical interconnects with high-bandwidth and low-latency properties. Furthermore, in order to adapt to application requirements, WDM technology can help the designer to improve ONoC characteristics, and, in particular, to increase the bandwidth and

to reduce the latency. However, using the WDM technology leads to the appearance of attenuation and crosstalk noise between the signals which are transferred on different wavelengths. Depending on the architecture of the ONoC and the structure of the Optical Network Interface (ONI), the value of crosstalk noise and attenuation can be different. In [71], the author present an analysis model of attenuation and crosstalk noise in ONoC with three different topologies: Mesh, Folded-torus, and Fat-tree. In [20], Duong *et al.* present the analysis of crosstalk based on the SUOR ring topology.

This chapter proposes an analytical model of attenuation and crosstalk noise for both device level and network level in a WDM-based ONoC which is discussed in the next section. To address these problems and explore the contribution regarding energy efficiency, we first give an overview of CHAMELEON architecture. Secondly, we present the fundamental analysis of the signal power attenuation and crosstalk noise at the device level. Based on the model at the device level and the architecture of the network, we develop an analytic model, providing the worst case of attenuation and crosstalk for different network sizes of the CHAMELEON's architecture. The models proposed in this chapter are used in Chapter 4 for energy efficiency optimization and in Chapter 5 for the design of the ONI manager unit.

3.2 Chameleon Architecture

Relying on the potential of optical interconnect properties with high bandwidth and low latency, ONoC is considered as one of the emerging solutions for future on-chip interconnects. In this section, we present a new version of ONoC architecture which is named CHAMELEON[1] [51] with three following features: a simple architecture, the optical network interface eases layout synthesis and run-time configuration, and various communication schemes. We step by step present these features in the following subsections.

3.2.1 Architecture Overview

Figure 3.1 illustrates the Chameleon architecture and its optical network interface (ONI). Chameleon consists of two layers: an electrical layer implementing the IP network and an optical layer performing the optical interconnect. The ONI is located between the

[1]CHAMELEON: Channel Efficient Optical Network-on-Chip – Lyon Institute of Nanotechnology

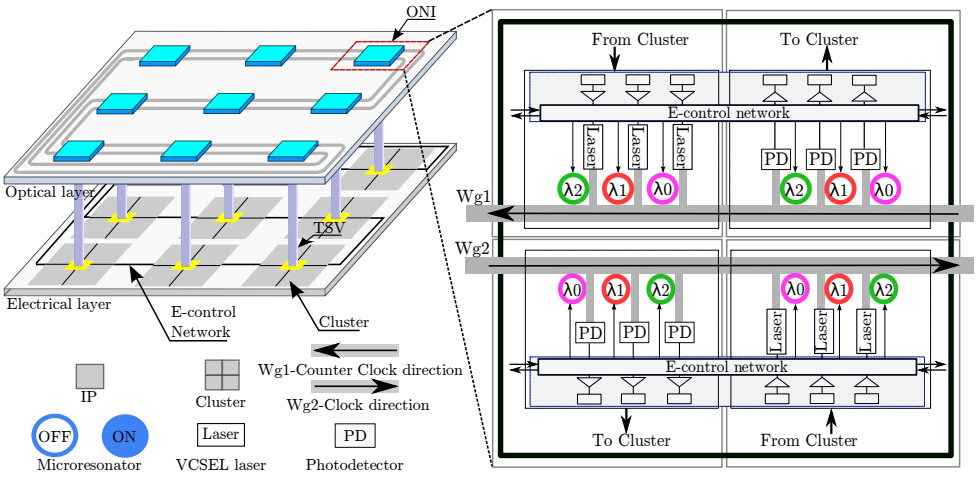


FIGURE 3.1: Chameleon optical interconnect and its Optical Network Interface (ONI)

optical layer and the electrical layer. It consists of ring-based waveguides and a set of optical components such as Micro-Resonators (MRs), on-chip laser sources, photo-detectors, TSV, ONI manager unit. To improve the scalability and the bandwidth of the channel, multiple waveguides are used in both directions (clockwise and counter-clockwise). By using multiple-waveguides, we can reduce the communication distance to minimize the worst-case of attenuation of ONoC. In the electrical layer, the unit management is implemented to configure the MRs and the laser power level according to communication requirements. Compared to the other existing ONoCs, one of the most potential features of CHAMELEON is the regularity of its architecture and the possibility of reconfiguration at run-time. Indeed, the most straightforward architecture of ONI can lead to the ease in layout synthesis, and the run-time configuration feature contributes to the higher energy efficiency. Moreover, the combination of the reuse of wavelengths and WDM technology can increase the bandwidth and reduce the power consumption of the overall system.

3.2.2 Optical Network Interface Architecture

In Chameleon, the ONI architecture is one of the most important factors that impact overall system performance. Each ONI is composed of a transmitter and a receiver, as described in Figure 3.2. The transmitter is composed of on-chip lasers and MRs, which operate as injectors (to inject the signal into the waveguide). The receiver part is composed of photo-detectors and MRs, which operate as ejectors (to drop the signal from the waveguide and guide it to the photo-detector). MRs are configured to be switched

ON or switched OFF by an ONI management network located in the electrical layer (see Chapter 5) to perform the three following operations.

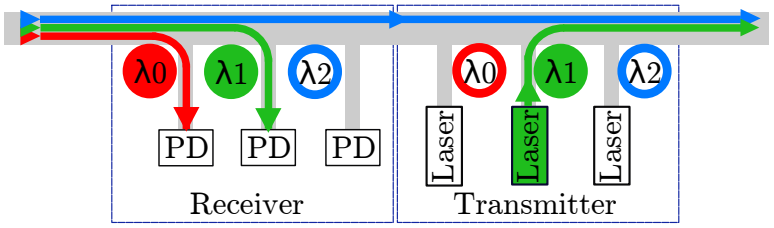


FIGURE 3.2: Illustration of the three operations in an ONI: injection, ejection and pass-through

- **Injection.** By turning ON the MR of the transmitter part, the light emitted by the laser is injected into the channel waveguide. The light then propagates until reaching another MR (at destination ONI) which extracts the light from the waveguide. Figure 3.2 illustrates the injection of a signal with wavelength λ_1 (in green color) into the waveguide.
- **Ejection.** Optical signals propagating along the waveguide cross the MRs at the receiver side. The signals, whose wavelength matches with the wavelength of ON state MRs, are dropped into the perpendicular (or parallel) waveguide and reach the photo-detector. Figure 3.2 illustrates the ejection of signals with wavelengths λ_0 and λ_1 from the waveguide (in red and green colors).
- **Pass-through.** In this case, all the MRs in the transmitter and the receiver parts are in the OFF state. An optical signal propagating along the waveguide will not be ejected, and no optical signal with the same wavelength will be injected for the sake of coherency and to avoid interference. Then, the signal crosses the ONI without being modified, as represented by the signal at wavelength λ_2 (in blue color) in Figure 3.2.

3.2.3 Communication Schemes

To support the communication requirements, an ONI manager can configure the MRs at run-time. Therefore, Chameleon provides many communication schemes corresponding to the application requirements: Single Writer Single Reader (SWSR), Single Writer Multi Reader (SWMR), Multi Writer Single Reader (MWSR), and High-Bandwidth Channel (HBC), as illustrated in Figure 3.3, Figure 3.4, Figure 3.5, and Figure 3.6.

SWSR (Single Writer Single Reader): By configuring the MRs, the point-to-point communication can be opened by using one or several wavelengths. Furthermore, by reusing one given wavelength, the channel partitioning can be obtained by performing multiple independent communications in the same waveguide. For instance, Figure 3.3 shows the point-to-point communications between: $ONI_A \rightarrow ONI_B$, $ONI_B \rightarrow ONI_C$ and $ONI_C \rightarrow ONI_A$ using λ_0 (in red); $ONI_C \rightarrow ONI_B$ using λ_1 (in green); $ONI_A \rightarrow ONI_D$ using λ_2 (in blue), respectively.

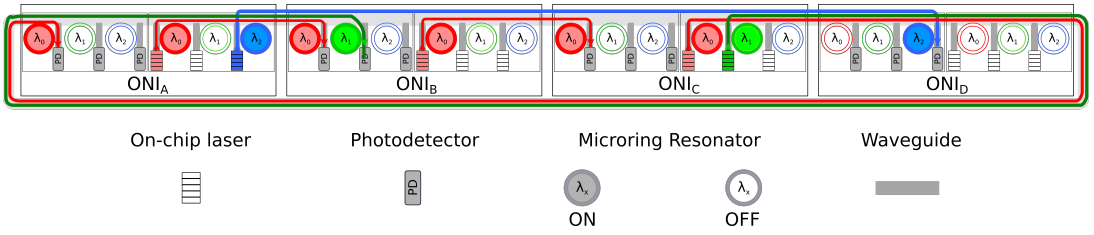


FIGURE 3.3: Single Writer Single Reader communication scheme

SWMR (Single Writer Multi Reader): This communication scheme can be implemented in Chameleon by allowing the communication between one ONI source and all the remaining ONIs. Figure 3.4 illustrates the SWMR communication between ONI_B with ONI_C, ONI_D, ONI_A by using λ_0 (in red), λ_1 (in green), λ_2 (in blue), respectively.

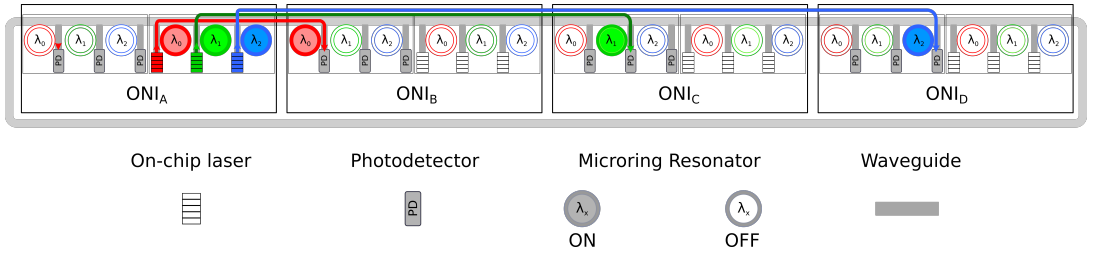


FIGURE 3.4: Single Writer Multi Reader communication scheme

MWSR (Multi Writer Single Reader): The MWSR communication scheme can be implemented by allowing the communication between several ONI sources and a given ONI destination. This communication scheme is illustrated by Figure 3.5 in which the ONI_A, ONI_B, and ONI_C respectively communicate with ONI_D by using λ_0 (in red), λ_1 (in green), λ_2 (in blue), respectively.

HBC (High-Bandwidth Communication): In this communication scheme, all of the wavelengths are allocated for a given communication. This feature can provide extra

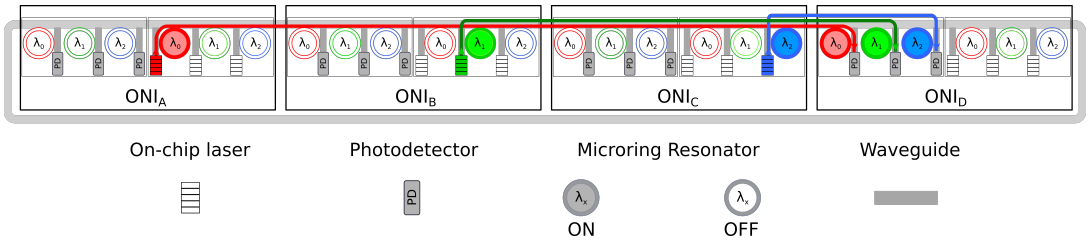


FIGURE 3.5: Multi Writer Single Reader communication scheme

high-bandwidth channel for a communication that may require the transmission of a large amount of data at a given time. As we can see in Figure 3.6, two high bandwidth communications (with the three wavelengths) are opened from ONI_B to ONI_D and from ONI_D to ONI_A, respectively.

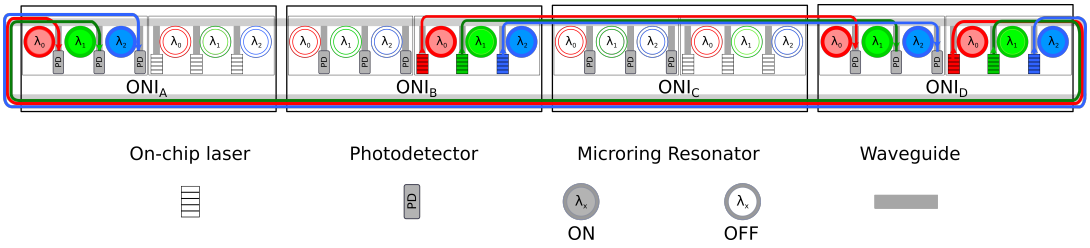


FIGURE 3.6: High-Bandwidth Communication scheme

Besides, multiple waveguides in both directions (clockwise and counterclockwise) are used to reduce the worst case of attenuation and to improve the channel bandwidth. Therefore, different communication schemes can be configured to adapt the communication requirements (Figure 3.7). This feature ensures high flexibility for Chameleon compared to other ONoC. However, it can lead to high complexity for the design of the ONI manager, and it can also increase the latency as well as the power consumption of the system. To make Chameleon more efficient, we need to consider the architecture exploration of the ONoC regarding power consumption and latency. To do this, the models of attenuation and crosstalk are primarily considered. In the next section, we analyse the optical attenuation and crosstalk noise at both the device level and system level.

3.3 Model of Attenuation

This section presents a model of the different communication losses in a 3D architecture integrating the CHAMELEON ONoC. The goal of this model is to provide a general platform for the exploration of energy efficiency properties in a 3D ONoC, as it will be

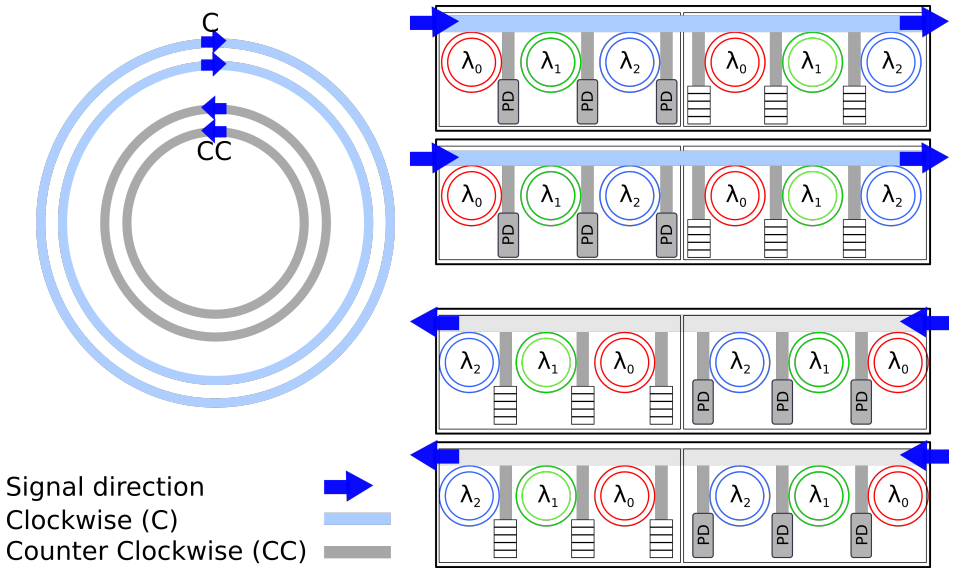


FIGURE 3.7: Bi-directional communication channels

discussed in Chapter 4 and Chapter 5. In order to provide this model, we first propose a fundamental analysis of losses and crosstalk noise at the device level. The study also takes the architecture, technology, and application parameters into account. Secondly, we analyze the worst case of attenuation and crosstalk noise of the architecture at the system level. Finally, some examples and results using this model are presented.

3.3.1 Fundamental Analysis

Crosstalk noise and loss are intrinsic problems of optical devices caused by the undesirable coupling among optical signals when they are transferred into a single waveguide. Crosstalk results in a small portion of the power of one signal leaking to other signals and thus becoming considered as noise with regards to the other signals. On the other hand, the evolution of optical technology has demonstrated that MRs are one of the WDM-compatible devices that are the most compact and energy efficient [66]. They are designed to resonate when presented with specific individual wavelengths and to remain quiescent in all other cases. These MRs are imperfect devices and they are the main source of crosstalk noise and attenuation loss.

In Chameleon, MRs with perpendicular configuration are used as injector/ejector to inject/eject the optical signal according to communication requirements. In this section, we focus on analyzing the loss and crosstalk in the MRs as injectors/ejectors.

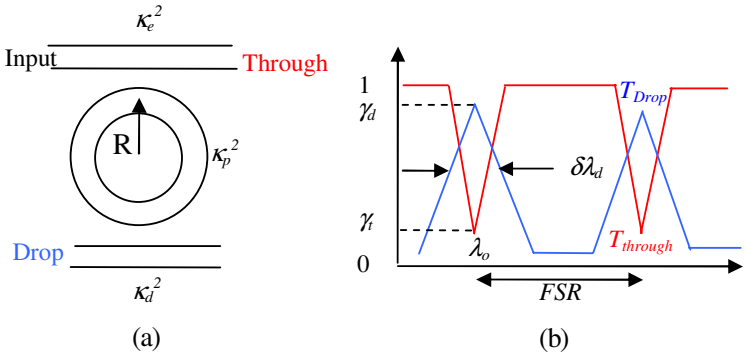


FIGURE 3.8: Theoretical model (a) and power responses (b) of a micro-resonator [115]

Figure 3.8 illustrates the theoretical model and the power resonance responses of an MR. In Figure 3.8.a, κ_e^2 and κ_d^2 are the fraction of optical power that the input waveguide and the drop waveguide couple into and out of the MR, respectively. κ_p^2 is a fraction of the inherent power losses per round-trip in the MR. R is the radius of the MR. Figure 3.8.b illustrates the power transmission responses of the MR. The power transmission response of through port and drop port are presented.

In this analytical model, MR is evaluated by Lorentzian power transfer function [114] peaked at the MR's resonant wavelength λ_j. For the signal in λ_i the power of signal at drop port can be calculated as

$$\frac{P_{drop}}{P_{in}} = \left(\frac{2\kappa_e\kappa_d}{\kappa_e^2+\kappa_d^2+\kappa_p^2}\right)^2 \frac{\delta^2}{(\lambda_i-\lambda_j)^2+\delta^2} \tag{3.1}$$

where the -3dB bandwidth of 2δ is expressed as $2\delta = \frac{\lambda_i}{Q}$ with Q is the Q-factor of a particular MR and λ_j is the center resonance wavelength of MR.

To simplify our analytical equations in the later stages, we assume that $\kappa_e^2 + \kappa_d^2 \gg \kappa_p^2$ and $\kappa_d \leq \kappa_e$. Therefore, $\left(\frac{2\kappa_e\kappa_d}{\kappa_e^2+\kappa_d^2+\kappa_p^2}\right)^2$ can be approximated to 1. We note the ratio $\frac{P_{drop}}{P_{in}}$ as $\Phi^D(i,j)$, which becomes

$$\Phi^D(i,j) = \frac{\delta^2}{(\lambda_i-\lambda_j)^2+\delta^2}. \tag{3.2}$$

Considering the Free-Spectral Range (FSR) of a signal as the difference between the MR's resonant wavelength λ_j and the examined signal wavelength λ_i, we have $\Delta(i,j) = \lambda_i - \lambda_j = (i-j)(\frac{FSR}{n})$, where we assume equal spacing between two consecutive wavelengths and n is the total number of wavelengths in the network. Furthermore, the power of signal at

input includes the power of signal at drop port and the power of signal at through port ($P_{in} = P_{Through} + P_{drop}$). Therefore, the power of through port can be determined by

$$\Phi^T(i,j) = \frac{P_{through}}{P_{in}} = 1 - \Phi^D(i,j). \tag{3.3}$$

Furthermore, the ON and OFF states of MR are represented in Figure 3.9. We can see

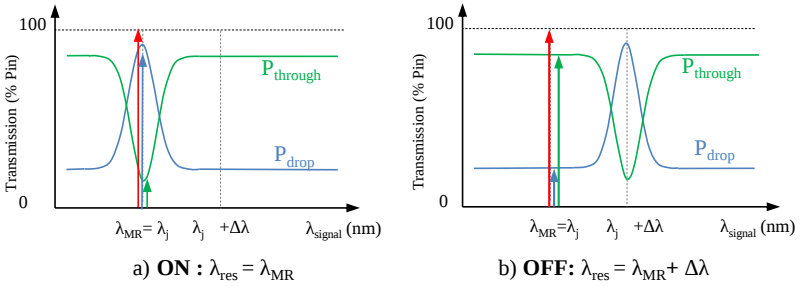


FIGURE 3.9: a) ON state and b) OFF state of MR [56]

that the state of MR corresponds to the resonant wavelength. According to [116, 45] with the thermo-optical method, when the resonance wavelength of MR is $\lambda_{MR} = \lambda_j$, the MR is turned ON. When the wavelength shifted to $\lambda_j + \Delta\lambda$, the MR is at OFF state. Based on this theory, we present the analytical eveluation of the crosstalk noise and loss at the device level and system level in the next sections.

3.3.2 Analyzing loss and crosstalk at device level

In Chameleon, the optical network interface is constructed by the active micro-ring with perpendicular configuration. This configuration is based on the advantage of multi-layer technology which has been introduced in Section 2.1.2.2. In the following section, we analyze the optical loss and crosstalk noise in MRs with the perpendicular configuration which is the basic optical element in Chameleon ONoC. There are two types of MRs in this configuration: the first one is the injector which is used to inject the signal from the laser source into the waveguide channel, and the second is the ejector which is used to drop the optical signal from the main channel into the photo-detectors.

3.3.2.1 MRs as perpendicular injector (Figure 3.10)

According to the Lorentzian transfer function, when the MR is OFF, the signal travels toward the drop port. In this case, the signal power in dB at the drop port when the MR

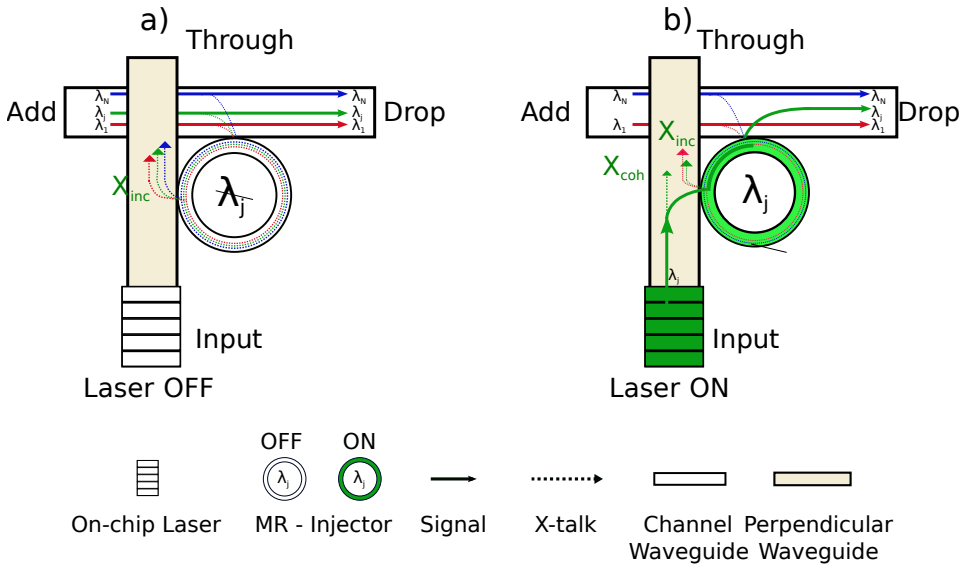


FIGURE 3.10: Analysis of perpendicular injector elements in (a) OFF-STATE and (b) ON-STATE

is OFF is

$$P_{s,D,OFF}(i) = P_{in}(i) + L_{inj-OFF}(\lambda_i, \lambda_j + \Delta\lambda) \qquad i = 0, 1, ..., n-1 \tag{3.4}$$

where $L_{inj-OFF}(\lambda_i, \lambda_j + \Delta\lambda)$ is the power loss of all signals passing through the injectors in OFF-state defined as

$$L_{inj-OFF}(\lambda_i, \lambda_j + \Delta\lambda) = \Phi^D_{dB}(\lambda_i, \lambda_j + \Delta\lambda) = 10\log_{10}(\Phi^D(\lambda_i, \lambda_j + \Delta\lambda)). \tag{3.5}$$

Because of the imperfection of the couplers, a portion of the light from all the wavelengths can leak into the perpendicular waveguide. This crosstalk noise (X_{inc}) is incoherent crosstalk and this does not have any effect on the photo-detector thanks to the perpendicular structure.

When the injector is turned ON, the signal of wavelength λ_j is injected to the channel. The MR is turned ON with wavelength λ_j, but it is turned OFF with all remaining wavelengths ($\lambda_i \neq \lambda_j$). Therefore, the signal power in dB at the drop port when the MR is ON is given by

$$\begin{aligned} P_{s,D,ON}(j) &= P_{Laser}(j) + L_{inj-ON}(\lambda_j, \lambda_j) \\ P_{s,D,ON}(i) &= P_{in}(i) + L_{inj-OFF}(\lambda_i, \lambda_j) \qquad (i \neq j) \end{aligned} \tag{3.6}$$

where $L_{inj-OFF}(\lambda_i, \lambda_j)$ is the loss of the optical signal with wavelength λ_i $(i \neq j)$ when

MR is at OFF-state (with λ_j) and $L_{inj-ON}(\lambda_j, \lambda_j)$ is the loss of the optical signal with wavelength λ_j when the MR is ON-state. These parameters are respectively expressed as

$$L_{inj-OFF}(\lambda_i, \lambda_j) = \Phi^D_{dB}(\lambda_i, \lambda_j) = 10\log_{10}(\Phi^D(\lambda_i, \lambda_j)) \tag{3.7}$$

and

$$L_{inj-ON}(\lambda_j, \lambda_j) = \Phi^D_{dB}(\lambda_j, \lambda_j) = 10\log_{10}(\Phi^D(\lambda_j, \lambda_j)). \tag{3.8}$$

When the light is coupled into the MRs, a portion of the optical signal from wavelength λ_j can go straight to the through port due to the imperfection of the couplers. Another imperfection is the incoherent noise which comes from other wavelengths which are leaking into the MRs and can also come to the through port. However, they do not have any impact to the photo-detector at the receiver thanks to the perpendicular structure and multi-layer technology.

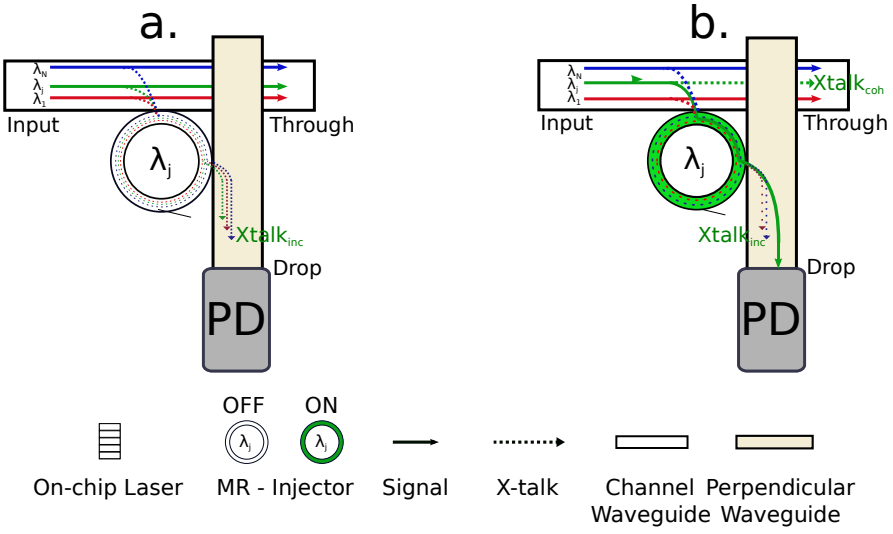


FIGURE 3.11: Analysis of perpendicular ejector elements in (a) OFF-STATE and (b) ON-STATE

3.3.2.2 MRs as perpendicular ejector (Figure 3.11)

For an ejector in the OFF-state, the signal travels toward the through port. According to the Lorentzian transfer function, the signal power in dB at the through port when the MR is OFF is

$$P_{s,T,OFF}(i) = P_{in}(i) + L_{eje-OFF}(\lambda_i, \lambda_j + \Delta\lambda) \qquad i = 0, 1, ..., n-1 \tag{3.9}$$

where $L_{eje-OFF}(\lambda_i, \lambda_j + \Delta\lambda)$ is the power loss of all signals passing through the ejectors in OFF-state defined as

$$L_{eje-OFF}(\lambda_i, \lambda_j + \Delta\lambda) = \Phi^T_{dB}(\lambda_i, \lambda_j + \Delta\lambda) = 10\log_{10}(\Phi^T(\lambda_i, \lambda_j + \Delta\lambda)). \tag{3.10}$$

Due to the imperfection of the coupling mode, a portion of light from all the wavelengths can leak into the perpendicular waveguide. This crosstalk noise power is incoherent and can be expressed as

$$P_{n-inc,D,OFF}(i) = P_{in}(i) + L_{eje-OFF}(\lambda_i, \lambda_j + \Delta\lambda). \tag{3.11}$$

For an ejector in the ON-state, the signal with wavelength λ_j is dropped into the photo-detector. Therefore, the signal power in dB at the through port when the MR is ON can be expressed as

$$P_{s,T,ON}(i) = P_{in}(i) + L_{eje-ON}(\lambda_i, \lambda_j) \qquad i \neq j. \tag{3.12}$$

The signal power in dB at drop port when the MR is ON is

$$P_{s,D,ON}(j) = P_{in}(i) + L_{eje-ON}(\lambda_j, \lambda_j), \tag{3.13}$$

where $L_{eje-ON}(\lambda_j, \lambda_j)$ is the power loss of signal with λ_j when passing through the ejectors in ON-state defined as

$$L_{eje-ON}(\lambda_j, \lambda_j) = \Phi^D_{dB}(\lambda_j, \lambda_j) = 10\log_{10}(\Phi^D(\lambda_j, \lambda_j)). \tag{3.14}$$

Due to the imperfection of the coupling mode, a portion of light from wavelength λ_j can leak to the through port. This crosstalk noise is coherent and its power is denoted by

$$P_{n-coh,T,ON}(j) = P_{in}(i) + L_{eje-ON}(\lambda_j, \lambda_j) \qquad i = 0, 1, ..., n-1 \tag{3.15}$$

where $L_{eje-ON}(\lambda_j, \lambda_j)$ is the crosstalk coefficient at ON-state of ejector, which represents the loss of signal power corresponding to the wavelength λ_j when dropped into the drop port, defined as

$$L_{eje-ON}(\lambda_j, \lambda_j) = \Phi^T_{dB}(\lambda_j, \lambda_j) = 10\log_{10}(\Phi^T). \tag{3.16}$$

Another crosstalk noise comes from other wavelengths which are leaked into the MRs and come to the drop port. This noise is incoherent crosstalk and is defined by

$$P_{n-inco,T,ON} = P_{in}(i) + L_{eje-OFF}(\lambda_i, \lambda_j) \qquad i \neq j \tag{3.17}$$

where $L_{eje-OFF}(\lambda_i, \lambda_j)$ is the signal loss coming from other wavelengths when passing through the MR ejector of wavelength λ_j in ON-state, defined as

$$L_{eje-OFF}(\lambda_i, \lambda_j) = \Phi^D_{dB}(\lambda_i, \lambda_j) = 10\log_{10}(\Phi^D(\lambda_i, \lambda_j)). \tag{3.18}$$

3.4 Signal to noise ratio and loss model at system level

This section presents the analysis of crosstalk and attenuation at the system level in the context of Chameleon ONoC. Due to the ring topology and layout properties of CHAMELEON with no waveguide crossing, the total attenuation in the optical path depends on

- the propagation loss in the waveguide L_{wg} (in dB),
- the bending loss L_b, and
- the injector/ejector loss.

The injector (ejector) loss $L_{injector}$ ($L_{ejector}$) in dB is based on the status of the MRs which can be ON-state or OFF-state. The total attenuation in the optical path is then

$$L_{total} = L_P + L_B + L_{injector} + L_{ejector}. \tag{3.19}$$

3.4.1 Propagation Loss

L_P is obtained from the intrinsic waveguide losses of the optical signal in the waveguide L_{wg} and from the distance d_{com} between the source and destination clusters.

$$L_P = L_{wg} \times d_{com}, \tag{3.20}$$

where L_P is the loss by signal propagation from source to destination cluster, L_{wg} in dB/cm is the loss of signal power when the signal is transferred in a 1 cm waveguide, d_{com} is the distance in cm of the considered communication from source to destination ONI.

This distance and all the estimations are derived automatically from the architecture by a Matlab program developed during this thesis.

3.4.2 Bending Loss

The bending loss L_B is the additional propagation loss when the waveguide is bent. For 90^o or 180^o bends, there are two sources of loss: bending loss and mode mismatch loss at the junctions between bending and straight waveguide. Bending loss depends on the bending radii and the loss with large bend radii is rather small. However, at system level, with a high number of bends, the bending loss must be considered as

$$L_B = N_b \times L_b, \tag{3.21}$$

where L_b is the loss of signal when passing through 90^o of bend and N_b is the number of bends along the communication.

3.4.3 Injector Loss

When a cluster sends the data to another cluster, the on-chip laser must be turned ON. Then, the light is emitted and injected into the channel and continues to propagate until reaching the destination ONI. Meanwhile, the MR-injector is in ON-state. Injector loss occurs in this mode of communication. The injector loss can be calculated as

$$L_{injector} = L_{inj-ON} \times N_{inj-ON} + L_{inj-OFF} \times N_{inj-OFF}, \tag{3.22}$$

where L_{inj-ON} and $L_{inj-OFF}$ are the loss of an injector in ON state and OFF state, respectively. These parameters are calculated based on the analytical model at the device level presented in Section 3.3.2. N_{inj-ON} and $N_{inj-OFF}$ are the number of injectors in ON-state and OFF-state along the communication.

3.4.4 Ejector Loss

When the light propagates along the channel to reach the destination ONI, signals whose wavelength matches with the resonance wavelength of microring will be ejected into the perpendicular waveguide and dropped on the photo-detector. Similar to the injector loss, the loss of signal in ejector can be defined as

$$L_{ejector} = L_{eje-ON} \times N_{eje-ON} + L_{eje-OFF} \times N_{eje-OFF}, \tag{3.23}$$

where L_{eje-ON} and $L_{eje-OFF}$ are the loss of an ejector in ON state and OFF state, respectively. These parameters are calculated based on the analytical model presented in Section 3.3.2. N_{eje-ON} and $N_{eje-OFF}$ are the number of ejectors in ON-state and OFF-state along the communication.

3.5 Simulation Results

In this section, we first present the parameters used in the model of attenuation and crosstalk which are due to the architecture and technology chosen. Then, simulation results for different sizes of Chameleon are shown. These results include the worst-case of attenuation and crosstalk used to improve the energy efficiency in the next chapters.

3.5.1 Technological and Architectural Hypotheses

In this section, we present an example with an architecture corresponding to 3×3 ONIs (see Figure 3.12). We use three wavelengths (λ_0, λ_1, λ_2) to implement the communication and two waveguides (clock and counter clock) for signal propagation. Furthermore, notations and values for parameters of the optical components used in this model are given in Table 3.1.

TABLE 3.1: Notations and value for parameters of the optical components

Parameter	Sym.	Value	Ref.
Propagation loss	L_p	-0.1dB/cm	[47]
Bending loss	L_b	-0.00215dB/90^o	[46]
Q-factor	Q	3383	[115]
Free-Spectral Range	FSR	15.74nm	[115]

To determine the impact of crosstalk noise in the optical interconnects, we use the SNR, the ratio between the received signal and the crosstalk noise power at the detectors.

3.5.2 Results and Analysis on the Proposed Model

In this section, we examine the communication between ONIs in the Chameleon architecture shown in Figure 3.12. By using the analytical model at the device level, we investigate the signal power loss and crosstalk noise of this architecture with 3×3 ONIs. Each ONI consists of a receiver and a transmitter. In the transmitter, three on-chip lasers (VCSELs) located in perpendicular waveguide emit three wavelengths (λ_0, λ_1, λ_2) which are injected to the waveguide channel by three MR injectors. In the receiver, three ejectors are used to drop out the signal whose wavelength matches with the MR wavelength resonances.

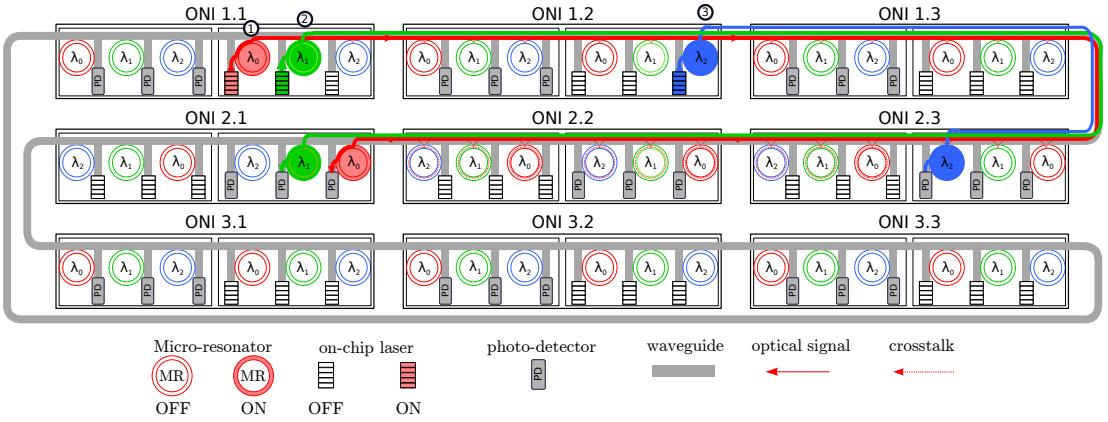


FIGURE 3.12: Chameleon ONoC with 3×3 ONIs and analysis of loss at system level

Figure 3.12 describes the example with 9 ONIs used in this section to illustrate how the model can be used to obtain the attenuation and crosstalk losses.. At a given time t_o, there are three parallel communication schemes corresponding to three markers ①, ② and ③. The first (①) is the connection between ONI 1.1 and ONI 2.1 using λ_0 (in red), the second (②) is the communication between ONI 1.1 and ONI 2.1 using λ_1 (in green), and the third (③) is the communication between ONI 1.2 and ONI 2.3 using λ_1 (in blue). We estimate the attenuation and crosstalk of the first communication by considering the impact of the second and the third communications. The laser signal corresponding to wavelength λ_0 passes through 4 ONIs from ONI 1.2 to ONI 2.2 and thus through 15 MR injectors and 13 MR ejectors. In each ONI, 3 MR injectors and 3 MR ejectors are turned ON to inject and eject the optical signal. Based on the analytical model developed at

the device level, we can derive the signal power with λ_0 at the photo-detector $PD1$ of ONI 2.1 as

$$P_{rx}(\lambda_0) = P_{Laser}(\lambda_0) + L_P(\lambda_0) + L_B(\lambda_0) + L_{injector} + L_{ejector}. \tag{3.24}$$

By applying the injector loss, ejector loss and the different parameters, the total attenuation becomes

$$\begin{aligned} P_{rx}(\lambda_0) &= P_{Laser}(\lambda_0) + L_P(\lambda_0) + L_B(\lambda_0) + L_{MR\text{-}ON} \times N_{MR\text{-}ON} + L_{MR\text{-}OFF} \times N_{MR\text{-}OFF} \\ &= P_{Laser}(\lambda_0) - (5 \times 0.5 \times 0.1 + 2 \times 0.00215 + 5 \times 0.0736 + 23 \times 0.0436) \\ &= P_{Laser} - 1.63(dB). \end{aligned} \tag{3.25}$$

The incoherent crosstalk noise is generated from signal with wavelengths λ_1 and λ_2, corresponding to communications ② and ③ happening in the same waveguide. This crosstalk noise is expressed as

$$P_{n\text{-}inc}(1) = P_{Laser}(\lambda_1) + L_P(\lambda_1) + L_B(\lambda_1) + L_{MR\text{-}ON} \times N_{MR\text{-}ON} + L_{MR\text{-}OFF} \times N_{MR\text{-}OFF} \tag{3.26}$$

and

$$P_{n\text{-}inc}(2) = P_{Laser}(\lambda_2) + L_P(\lambda_2) + L_B(\lambda_2) + L_{MR\text{-}ON} \times N_{MR\text{-}ON} + L_{MR\text{-}OFF} \times N_{MR\text{-}OFF}. \tag{3.27}$$

3.6 Conclusions

In this chapter, we present the analytical models of loss and crosstalk noise in the optical network-on-chip. In our model, both the losses and crosstalk noises are carefully analyzed at two levels: device level and system level. First, we analyze the loss and crosstalk at the device level with the transmission function of the micro-ring resonator. Based on the device level, we explore the architecture of Chameleon ONoC and provide the analyses of the worst case of loss and crosstalk noise. By using this model, we can provide a generic

analysis of attenuation and crosstalk among various parameters of an optical network-on-chip. This result will be used to provide in the next chapter to estimate the power consumption of optical interconnects.

Chapter 4

Error Correction Codes for Energy-Efficient Optical Interconnects

In on-chip optical interconnects, there are two main major issues contributing to overall system performance: Energy Efficiency and Bit Error Rate (BER). Unfortunately, for the definition of an optical interconnect, these two elements evolve in opposite directions: to reduce the BER, we need to increase the power of the laser, which will increase the energy consumption of the optical link.

Furthermore, due to errors created by the thermal effect onto the MRs as well as errors occurring during the optical signal transmission, the reliability and energy efficiency of communication channels can be decreased. Especially, in complex MPSoCs composed of hundreds of cores, reliability and energy are major challenges requiring a lot of effort to be solved. In this chapter, we propose a new method based on Forward Correction Codes (FEC) to improve the reliability and the energy efficiency of a communication channel by exploring the trade-off between the laser power and the quality of the communication (BER).

This chapter is organized as follows. Section 4.1 presents the introduction and the related work. Section 4.2 presents the approach we propose to address this issue. Section 4.3 illustrates the channel modeling and energy/performance trade-offs. The problem

formulation and FEC's evaluation are presented in Section 4.4. Section 4.6 shows the results and their analysis. Finally, Section 4.7 concludes this chapter.

4.1 Problem Statement

Recently, reliable optical interconnects with high bandwidth and low latency can be obtained by using the Wavelength Division Multiplexing (WDM) technology. In WDM, micro-ring resonators (MRs) are used to modulate, switch, inject and extract the optical signal. However, these MRs are one of the main components introducing crosstalk noises and power losses [71] during communications. These losses degrade system performance via the reduction of Signal to Noise Ratio (SNR). This chapter aims to improve the energy efficiency of the system by using some coding techniques. The problem statement and the proposed approach are illustrated in Figure 4.1 where a point-to-point optical communication between the source IP (IP_{TX}) and the destination IP (IP_{RX}) is illustrated. The left side of Figure 4.1 shows the transfer function of the transmitted laser power which can be modulated by the micro-ring modulator. In Figure 4.1.a, the laser power is set to its maximum value (P_A) in order to reach a given bit error rate BER_A. At the receiver side, the optical signal is detected by a photodetector. The signal is reduced due to the losses during the propagation on the optical waveguide (see Chapter 3). Furthermore, the signal is also noisy due to crosstalk between other optical signals on the waveguide. These two effects reduce the Signal-to-Noise Ratio SNR_A. The amount of laser power during transmission is directly linked to SNR_A and is represented by the bit error rate BER_A. Figures 4.1.d and 4.1.e illustrate the plots of energy and BER versus communication time.

In order to reduce the power consumed, there are two possibilities. The first one is the straightforward method in which the power of the laser is reduced to decrease power consumption. Figure 4.1.b illustrates this solution with a small laser power (P_B). At the receiver side, the signal is attenuated with the same loss, but crosstalk noise is not reduced. Hence, as the laser power is reduced, the SNR_B is lower than SNR_A. The operating point of this state is represented by point Ⓑ in Figures 4.1.d and 4.1.e. However, reducing the SNR_B for a communication can lead to a BER_B out of the acceptable BER for this communication link.

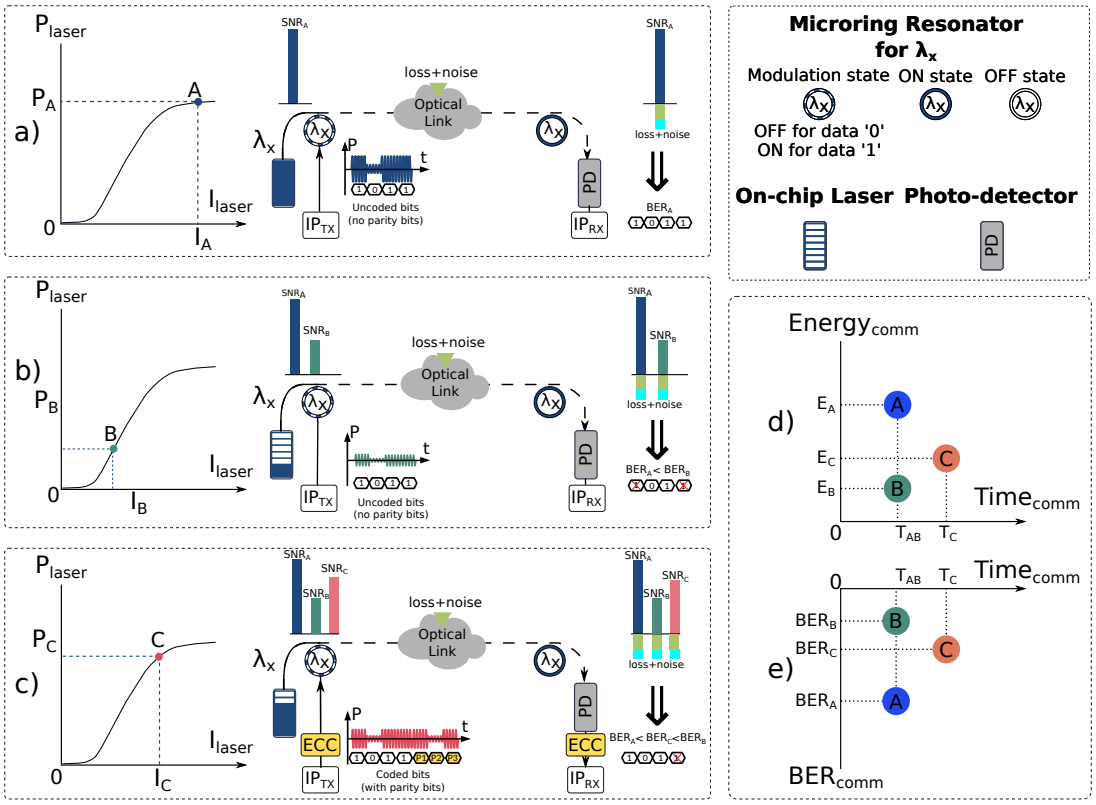


FIGURE 4.1: Impact of laser power on energy and latency for a point-to-point communication.

The second solution to reduce power consumption of this communication is the integration of error correction codes (ECC), as presented in Figure 4.1.c. This figure illustrates the communication with the integration of ECC in the electronic layer. In this case, the power of laser P_C is less than P_A. However, by adding some redundant bits to the information bits, ECC can improve the BER of the communication. Then, if we target a specific BER, we can reduce the laser power. This method is represented by the operating point Ⓒ in Figures 4.1.d and 4.1.e with higher performance in terms of energy and BER (BER_C) compared to the first approach. Then, this method can be interesting in terms of energy efficiency. However, it also introduces an overhead in communication latency time, due to ECC computation delay. Figure 4.1.d and Figure 4.1.e show the relation of the Energy and BER versus communication time. The communication time of the system with ECC (point Ⓒ) is higher than the system without ECC (Ⓐ and Ⓑ), but it can be used to reduce the power consumption while ensuring the required communication quality.

4.2 Proposed Approach

ECC is one of the key-enabling elements to enhance the reliability and the energy efficiency in on-chip optical interconnects by reducing the error probability during the transmissions. There are two main approaches using ECC. The first approach, called ARQ (Automatic Repeat Request or Automatic Repeat Query), is an error-control method for data transmission, relying on the re-transmission of the messages until the errors disappear. The second approach is FEC (Forward Error Correction), an error-control technique in data transmission over unreliable communication channels [72] which adds some redundancy bits to the information bits and corrects them at the receiver side by a decoder.

During data transmission, some errors can arrive due to the sensitivity of optical filters and optical switches as weel as to crosstalk noise and thermal issues. For ARQ protocol, the re-transmission is very complex due to the need of feedback communication. It leads to an increase in latency in optical interconnects and also consumes power to support the re-transmissions of the data. Another solution is the combination of ARQ and FEC. However, this technique can increase the latency as well as the implementation complexity. In this context, FEC is an exciting solution which can be used to reduce the global power consumption and to improve the reliability of the communication channel.

As mentioned in Chapter 2, there exists a lot of FEC techniques used in Wireless Sensor Networks (WSN) and in optical communications [36, 100, 107]. However, in order to determine which solution is the best suited FEC technique for on-chip optical interconnect environment, we have to take some of their properties into account, in particular regarding bandwidth and latency. On-chip nanophotonics interconnects are composed of on-chip laser sources, micro-ring resonators (MRs), waveguides and photo-detectors. Compared to traditional electrical interconnects, the optical devices are more power hungry. By considering this problem, new approaches to share the power consumption between the electrical and optical domains are needed to reduce the global power consumption.

This chapter addresses this challenge and proposes to add data protection in the electrical domain, which allows for the reduction of the power consumption of optical transmission without any reduction of the communication quality. For this purpose, FEC encoders are used on the transmitter side, and faulty bits are detected by the receiver and corrected.

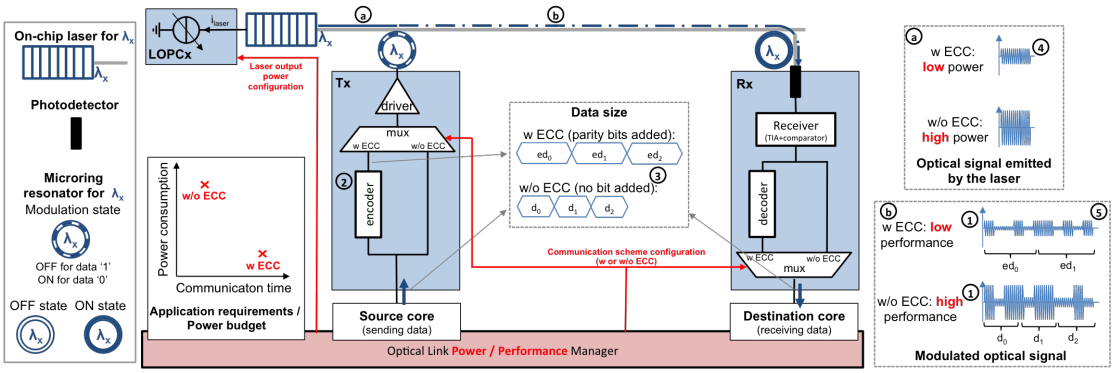


FIGURE 4.2: General principle of the use of ECC in an ONoC [43]

Since additional faulty bits are acceptable using FEC, the optical power emitted by the laser source can be significantly reduced. The laser having a significant contribution to the power consumption, the global power of the optical interconnects can therefore be significantly reduced under specific scenarios without compromising the energy-per-bit figures.

4.3 Point-to-point Link and Energy/Performance Trade-offs

Figure 4.2 illustrates our approach in the context of a simple optical link with one laser source, one writer (source core) and one reader (destination core). We first detail the basic communication schemes without ECC. Then, we revisit the transmission schemes when ECC is used.

4.3.1 Communication Without ECC

To communicate, the source core i) sets the corresponding MR to the modulation state and ii) sends the data (d_0, d_1 and d_2 in the figure). The data are serialized, and the corresponding stream of information bits leads to an On-Off-Keying (OOK) modulation of the optical signal at the wavelength λ_x, which is emitted by the laser. The modulation is realized by the electro-optic effect on the MR. Forward bias is applied to perform voltage tuning, which leads to a blue shift of the MR resonant wavelength. In our model, data '1' and '0' lead to OFF state and ON state, respectively:

- OFF state: the MR resonant wavelength is detuned from the optical signal and the optical signal continues propagating with low losses.

- ON state: the MR resonant wavelength and the optical signal are aligned. Most of the optical signal power is absorbed by the MR, which leads to a strong attenuation on the output.

The difference between OFF and ON attenuations defines the extinction ratio. As an example, a 9.2dB extinction ratio at 9Gb/s with 4.32mW and for a 2Vpp CMOS driver has been reported in [55]. In Figure 4.2, this is illustrated by the gap between the two optical signal power levels (marked as ①). The modulated signal then propagates along the waveguide until the receiver, where it is dropped to the photodetector (the optical signal is dropped by MR, by putting it in ON state). The photocurrent is then converted back to a digital data transmitted to the destination core. The transmission can be characterized as follows:

- Power: during the transmission, the modulated optical signals experience losses (not shown in the figure but discussed later on). The laser thus must emit a high enough optical power in order to reach the targeted BER (e.g. 10^{-9}), knowing the losses, the MR extinction ratio, and the photodetector dark current. Because the laser efficiency is relatively low (e.g. around 5%), its contribution in the optical link power budget is significant.
- Performance: thanks to the direct modulation of the data (i.e. without ECC), the transmission time is reduced to the minimum if the target BER is reached.

The following section discusses how the use of ECC impacts the optical communications.

4.3.2 Communication With ECC

When an ECC is included in the communication link, the data to be emitted are first encoded (ed_0, ed_1 and ed_2 in Figure 4.2, marked as ②) before serialization and modulation. Due to the added bits to be transmitted, the communication time is longer (marked as ③). In the receiver, the optical signal is converted back into electrical signal, and the data are decoded. This receiver allows for detecting and correcting errors, which in turns improves the BER. Hence, assuming the same target BER as for the communication without ECC, the constraints on the SNR are leveraged when ECC is used. This leads to reducing the power of the optical signals, as suggested in the figure with the decreased

amplitudes of the emitted signal (marked as ④) and the modulated signal (marked as ⑤). It is worth mentioning that the extinction ratio is the same. Hence, a global reduction of the optical link power is achievable if the energy saved on the laser side is larger than the energy consumed in the data coding/decoding and the transmission of the added bits.

4.3.3 BER and Laser Power Trade-Offs

In short, without ECC, communications are fast, but the power needed to ensure quality (specific BER) can be important. At the opposite, with ECC, the communication time is increased but the power consumption is potentially reduced, and the communication can be more efficient. This complementary trend well suits execution constraints of nowadays applications running on complex MPSoCs. Although execution deadlines have to be met for real-time applications, energy saving strategies can be applied for power-hungry multimedia-like applications (e.g., by degrading the BER).

This chapter presents how to configure nanophotonics interconnects by jointly i) selecting the ECC used for data transmission and ii) tuning the laser output power. Hence, by considering i) application requirements and power budget and ii) ECC performance and power figures, a manager configures at run-time the optical link. The configuration is two-fold: First, the most appropriate communication scheme with or without ECC (w ECC or w/o ECC in the figure) is selected, and both writer and receiver are configured accordingly; Second, the optical power of the signal emitted by the laser is set in order to respect the BER requirement which is achieved by tuning the laser current.

The use of a shared or centralized manager to configure one ONI emitter and one ONI receiver is a standard solution in ONoCs [112]. In this type of architectures, a source sends a request to the manager by specifying the destination and the communication requirements and the manager responds with the suitable configuration to apply on both source and destination sides. Hence, adding the communication scheme (with or without ECC) within the responses has a limited impact on the manager cost (this problem is addressed in Chapter 5). The choice of the communication scheme is handled by the Operating System (OS) through evaluation of losses due to other communications in the waveguide.

4.4 Power and Energy Saving in Optical Interconnects

Energy is one of the important factors impacting overall system performance of ONoC. To determine the impact of FEC to the optical interconnects as well as the trade-off between the energy saving and the BER, we must consider the power budget which consists of the transmitted laser power, the power consumption of FEC, the photo-detector sensitivity and the optical losses.

4.4.1 Transmitted Laser Power

In optical network-on-chip, to ensure a "correct" communication (with the required BER), the transmitted laser power must be adapted to be sure that a minimum power level is received on the photo-detector [111]. This BER condition is linked to the ratio between signal and noise powers. If the power of the received signal at the photo-detector is too small, the optical link will operate unreliably. The signal to noise ratio at the photo-detector is defined as

$$\frac{S}{N} = \frac{R.E_b}{B.N_0} = k\frac{E_b}{N_0}, \tag{4.1}$$

where R is the information bit rate (in bits per second), E_b the energy per bit (in Joules per bit), B the signal bandwidth, N_0 the noise power spectral density, and k the spectral efficiency (ratio of the information rate to the bandwidth).

Additionally, the power S of the signal arriving at photo-detector is given by

$$S = PO_{Laser} - L_{optic}, \tag{4.2}$$

where PO_{Laser} is the transmitted laser power in dBm and L_{optic} is the total loss of optical components during the optical communication from the transmitter ONI to the receiver ONI. This loss value can be extracted from the model of loss which was already provided before in [83] (see Chapter 3)

From Equations 4.1 and 4.2, we can write

$$\begin{aligned} PO_{Laser} &= L_{optic} + \frac{S}{N}N \\ &= L_{optic} + k\frac{E_b}{N_0}N \end{aligned} \tag{4.3}$$

where N is the power of noise at the photo-detector.

4.4.2 Power and Energy-per-Bit Saving

Using ECC allows for a coded system to operate at lower SNR than the uncoded system at a given BER. This section presents the power and energy-per-bit saving due to the lowered transmitted power in terms of the power consumption in the ECC codecs.

4.4.2.1 Communication Without ECC

For uncoded communication, at a given BER, the minimum required laser power $PO_{Laser,U}$ (in Watt) to achieve SNR_U at the photo-detector is

$$\begin{aligned} PO_{Laser,U} &= 10^{L_{optic}/10} \times k_U \frac{E_b}{N_0} N \\ &= 10^{L_{optic}/10} \times k_U 10^{SNR_U/10} N \end{aligned} \tag{4.4}$$

where $k_U = R/B$ is the uncoded spectral efficiency and SNR_U is the required signal to noise ratio in dB of the uncoded communication.

One of the main factors significantly contributing to the optical link power budget is the laser efficiency ($Laser_{eff}$) as it could be very low (e.g. 5%). The meaning of this parameter is that the cost of any additional Watt for the laser in the optical domain requires more 20 times power in the electrical domain to drive the laser. Then the electrical power (in Watt) to drive the laser during a communication without ECC is

$$\begin{aligned} PE_{Laser,U} &= \frac{PO_{Laser,U}}{Laser_{eff}} \\ &= \frac{10^{L_{optic}/10} \times k_U \times 10^{SNR_U/10} \times N}{Laser_{eff}}. \end{aligned} \tag{4.5}$$

4.4.2.2 Communication With ECC

For the communication with ECC, the minimum transmitted laser power (in Watt) to obtain the target SNR_C at the photo-detector is

$$\begin{aligned} PO_{Laser,C} &= 10^{L_{optic}/10} \times k_C \frac{E_b}{N_0} N \\ &= 10^{L_{optic}/10} \times k_U 10^{SNR_C/10} N \end{aligned} \tag{4.6}$$

where $k_C = R/B_C$ is the coded spectral efficiency and $SNR_C = E_b/N_0$ is the required signal to noise ratio in dB of the coded communication.

Similarly, the electric power required to drive the laser during a communication with ECC is

$$\begin{aligned} PE_{Laser,C} &= \frac{PO_{Laser,C}}{Laser_{eff}} \\ &= \frac{10^{L_{optic}/10} \times k_C \times 10^{SNR_C/10} \times N}{Laser_{eff}} \end{aligned} \tag{4.7}$$

4.4.2.3 Power Saving Using ECC in Optical Interconnects

For a fair comparison, the communication with ECC must show the same information rate R as the uncoded communication. As we can see in Figure 4.3, after encoding, the number of bits of the codeword is greater than the number of information bits $(N > K)$ due to the addition of M redundancy bits. Then, it is unfair to compare the two schemes if the communication with ECC has the same transmission rate. In this case, the information bit rate will be decreased to $R.R_C$, with R_C the ratio between some information bits and codeword bits ($R_C = K/N$). This means the uncoded communication decodes R information bits while only $R.R_C$ information bits are decoded in ECC communication. Therefore, the uncoded communication and the communication with ECC must have the same information transmission rate. As a result, the coded transmission rate increases to $R_n = R/R_C$ and the coded communication bandwidth is $B_C = R_n$.

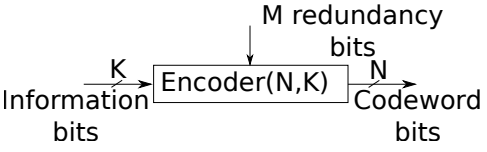


FIGURE 4.3: Size of input and output data for communication with ECC (N,K) encoder

From Equations 4.5 and 4.7, we can write

$$\frac{PE_{Laser,U}}{PE_{Laser,C}} = \frac{K_U}{K_C} 10^{ECCgain/10} \tag{4.8}$$

where

$$ECC_{gain} = SNR_U - SNR_C \tag{4.9}$$

is the coding gain when ECC is used. Then, Equation 4.8 can be rewritten as

$$\begin{aligned} PE_{Laser,C} &= \frac{K_C}{K_U} \frac{PE_{Laser,U}}{10^{ECC_{gain}/10}} \\ &= \frac{B}{B_C} \frac{PE_{Laser,U}}{10^{ECC_{gain}/10}}. \end{aligned} \tag{4.10}$$

Finally, from Equations 4.5, 4.7 and 4.10, the **power saving** in Watt of the communication by using ECC (N, K) codecs is

$$\begin{aligned} \Delta P_{save} &= PE_{Laser,U} - PE_{Laser,C} - P_{codecs} \\ &= \frac{PO_{Laser,U}}{Laser_{eff}} \left(1 - \frac{B}{B_C} \frac{1}{10^{ECC_{gain}/10}}\right) - P_{codecs} \end{aligned} \tag{4.11}$$

where $PO_{Laser,U}$ (in Watt) is the minimum transmitted laser power of the uncoded communication and P_{codecs} is the power consumption of the ECC encoders and decoders. Furthermore, the minimum transmitted power of laser can be directly determined from the photo-detector sensitivity, such as

$$PO_{Laser,U}(dBm) = P_{sen}(dBm) + L_{wc}(dB) \tag{4.12}$$

where $P_{sen}(dBm)$ is the sensitivity of the photo-detector and $L_{wc}(dB)$ the worst-case of losses of the system. These parameters will be carefully discussed in the next section.

Finally, the power saving of the communication (in milliWatt) can be written as

$$PO_{Laser,U} = 10^{\frac{PO_{Laser,U}(dBm)}{10}}. \tag{4.13}$$

4.4.2.4 Energy-per-Bit Saving Using ECC

The required transmit energy per information bit is determined by dividing the required transmit power P_{TX} by the transmission information rate R:

$$E_{TX} = \frac{P_{TX}}{R} \quad (J/bit). \tag{4.14}$$

For the communication without using ECC, the minimum transmitted energy per bit is

$$E_{b,U} = \frac{PE_{Laser,U}}{R} \quad (J/bit). \tag{4.15}$$

Similarly, for the communication with ECC, the minimum transmitted energy per bit is

$$\begin{aligned} E_{b,C} &= \frac{PE_{Laser,C}}{R} \\ &= \frac{B}{B_C}\frac{E_{b,U}}{10^{ECC_{gain}/10}} \quad (J/bit). \end{aligned} \tag{4.16}$$

The energy cost per information bit for the encoder and the decoder could be expressed as

$$Eb_{codecs} = \frac{P_{encoder} + P_{decoder}}{R} \quad (J/bit) \tag{4.17}$$

where R is the information bit ratio. Therefore, from Equations 4.15, 4.16 and 4.17, the **total energy saving using ECC** to ensure the communication properly operate at a given BER is

$$\begin{aligned} \Delta E_{save} &= E_{b,U} - E_{b,C} - E_{codecs} \\ &= E_{b,U}\left(1 - \frac{B}{B_C}\frac{1}{10^{ECC_{gain}/10}}\right) \quad (J/bit). \end{aligned} \tag{4.18}$$

4.4.3 Sensitivity of the Photo-Detector

To obtain the minimum power of laser (dBm), we should know the sensitivity of photo-detector $P_{sen}(dBm)$ and the worst case of losses of the communication path. As discussed in the previous chapter, the worst case of loss depends on the following parameters of the ONoC architecture: number of wavelengths per waveguide, channel distance ($\Delta\lambda$), allocated wavelengths, number of IPs, length of the waveguide and distance between two neighbouring optical network interfaces. This latter parameter is a significant factor

contributing to the energy efficiency of the overall system. Indeed, at a given BER and photo-detector sensitivity, the worst case loss is directly proportional to the minimum laser power. These parameters can be extracted from the model of losses developed in the previous chapter.

The photo-detector is the optical device which converts the optical signal into the electrical signal. In order to ensure the optical interconnects to operate properly at a given BER, the received signal power should not be lower than the photo-detector sensitivity $P_{sen}(dBm)$, which gives

$$P_{Laser,min} - L_{wc} \geq P_{sen} \tag{4.19}$$

where $P_{Laser,min}(dBm)$ is the minimum transmitted laser power and L_{wc} is the total loss between sender and receiver.

There are two kinds of photo-detectors usually used for optical communications: PIN photo-detector and APD photo-detector (the avalanche photo-diode). However, PIN photo-detector is the most often implemented receiver in optical interconnects [44]. Anyway, in both cases, the sensitivity of the photo-detector is computed as

$$P_{sen} = 10\log\left[1000 \times \frac{OMA(r_e+1)}{2(r_e-1)}\right](dBm) \tag{4.20}$$

where r_e is the extinction ratio of the received optical signal and OMA the optical modulation amplitude defined as the difference between the power levels representing a logic one (P_1) and logic zero (P_0). OMA can be expressed as

$$OMA(\mu W) = i_n \times SNR/\rho \tag{4.21}$$

where responsivity ρ is the conversion efficiency of the photo-detector in Amperes per Watt (A/W) and input-referred noise i_n is the noise floor of the transimpedence amplifier (in A_{RMS}). These values can be extracted from the device parameters of the transimpendence amplifier part. The signal to noise ratio SNR is the peak-to-peak signal to noise ratio. This value can be obtained by the error probability function of the system.

Assuming a 10 Gbps receiver with typical input-referred noise of $1.1\mu A_{RMS}$, photo-detector responsivity of $\rho = 0.85(A/W)$ and extinction ratio of $r_e = 6.6$, the evaluation of photo-detector sensitivity is shown in Figure 4.4.

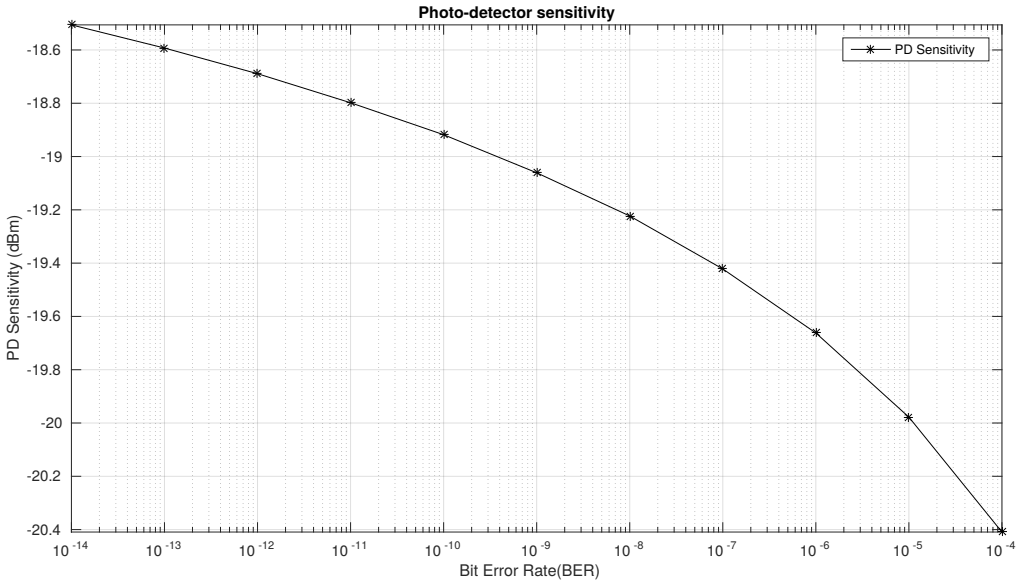


FIGURE 4.4: Sensitivity of a photo-detector shown for 10 Gbps with $i_n = 1.1\mu A_{RMS}$, $r_e = 6.6$ and $\rho = 0.85(A/W)$.

4.4.4 Trade-off Between BER and FEC Coding Gain

Figure 4.5 illustrates an optical interconnect without the encoder and decoder, assuming that bits passing through the channel suffer from independent noise. Without coding technique, the error probability function of the channel in terms of OOK modulation is expressed as

$$P_U = Q(\sqrt{SNR}) \tag{4.22}$$

where Q(x) is the Q-function of errors.

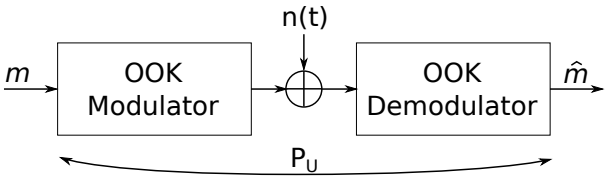


FIGURE 4.5: Optical interconnect without ECC

When the t-error correcting code is used, all the errors which are less than or equal to t will be corrected by the decoder. In this case, the error probability function of the ECC can be generalized as

$$P_B = \frac{1}{n} \sum_{j=t+1}^{n} j\binom{n}{j} P_U^j (1 - P_U)^{n-j}. \tag{4.23}$$

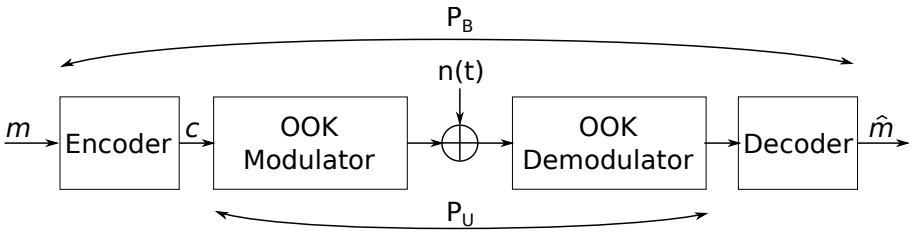


FIGURE 4.6: The optical interconnect with ECC

As discussed in the previous chapter, Hamming codes and Reed-Solomon codes have demonstrated their ability to become candidates for on-chip optical interconnects [99, 86]. The error probability functions of Hamming(n,k) with OOK modulation technique are given by

$$P_B = P_U - P_U(1-P_U)^{n-1} \tag{4.24}$$

where n is the length of codeword, m is the number of the redundant bits and k is the length of data input $k = n - m$.

The error probability of Reed-Solomon code RS(n,k,d) is

$$P_B = \frac{2^{q-1}}{2^q-1}\frac{1}{n}\sum_{j=t+1}^{n} j\binom{n}{j}P_U^j(1-P_U)^{n-j}. \tag{4.25}$$

Based on the analyzed equations, BER performance of Hamming$(7,4)$, Hamming$(71,64)$ and RS$(15,11,5)$ is illustrated in Figure 4.7. In this figure, the difference in E_b/N_0 (or SNR) to achieve a given BER of a given codec compared to the uncoded version is called coding gain. At $BER = 10^{-12}$, the corresponded SNR of the channel with RS$(15,9,6)$, H$(7,4)$, H$(71,64)$ and uncoded (points a, b, c, and d in the figure) are 12.11, 14.26, 13.85 and 16.94 dB, respectively. The chart of Figure 4.8 shows that at $BER = 10^{-12}$, the RS$(15,11,5)$ code provides the best performance in coding gain with 4.83 dB compared to the other codecs. However, each codec comes also with a different hardware complexity of the error correcting algorithm. Therefore, to make a fair comparison in terms of power saving and energy saving between the different ECC methods, we must consider the power consumption and the hardware cost needed for the encoders and decoders. This point is discussed in the following section.

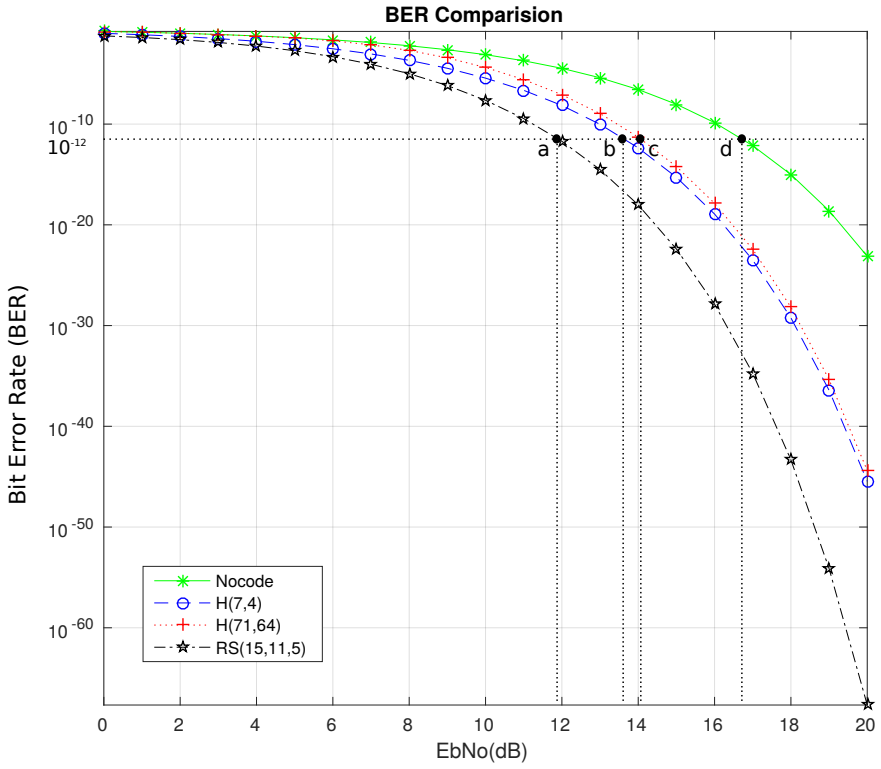


FIGURE 4.7: BER versus E_b/N_0 of Hamming$(7,4)$, Hamming$(71,64)$ and RS$(15,11,5)$

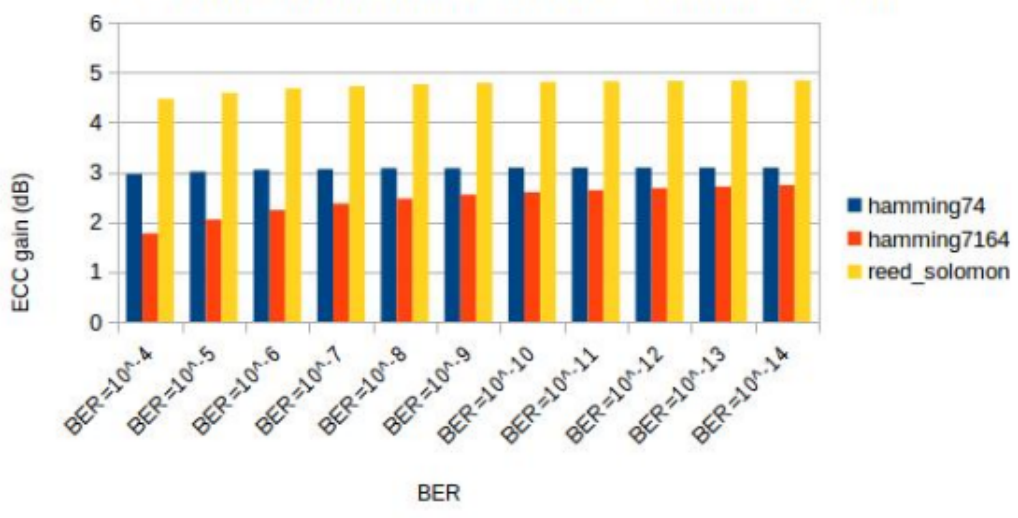


FIGURE 4.8: ECC gain comparison on energy for H(7,4), H(71,64), and RS(15,11,5)

4.5 Hardware Evaluation of ECC Techniques

Using error correcting codes can reduce the minimum laser power needed for a communication due to the coding gain. However, we also need to consider the power consumption consumed by the encoders and decoders (P_{codecs}). Power consumption consists of static power and dynamic power. Static power (due to leakage current) P_s depends on the state of the inputs, temperature, process and voltage. P_s can be modelled as

$$P_s = I_{leak}.V \tag{4.26}$$

where V is the voltage supply and I_{leak} the leakage current. Dynamic power consumption P_d is composed of internal power and switching power and can be modelled as

$$P_d = C.V^2.f \tag{4.27}$$

where C is the total switched capacitance and f the frequency. Therefore, the total power consumption is

$$P_t = P_d + P_s = C.V^2.f + I_{leak}.V \tag{4.28}$$

To estimate the power consumption of encoder and decoder blocks, each hardware component was designed using Verilog and synthesized using Synopsys Design Vision for a 28nm FDSOI technology. Power metrics were calculated by back annotating the switching activity of internal nets and then importing files in the Synsopys PrimeTime tool. Clock gating was applied and energy-per-bit was computed by assuming 50% switching activity of the inputs.

Table 4.1 shows the power consumption of the following codec H(7,4), H(71,64) and RS(15,11,5) and provides static, dynamic and total power reports. The lowest power consumption is for Hamming(7,4) due to its simple implementation. Because of the larger data size, the power consumption of H(71,64) is higher than for Hamming (7,4). Figure 4.7 shows that RS(15,11,5) has the best performance in coding gain. However, it also consumes the highest power with 13.1 μW due to the complexity of decoding algorithm. In order to know which codec is the best candidate in energy and power efficiency, the energy and power saving will be evaluated at the system level in the next section.

TABLE 4.1: Power consumption results for simple Hamming and Reed Solomon ECC blocks

ECC	Static Power (nW)	Dynamic Power (μW)	Total Power (μW)
H(7,4)	0.268	0.433	0.434
H(71,64)	3.960	4.960	5.160
RS(15,11,5)	43.58	12.99	13.10

4.6 Power and Energy Saving using ECC in Optical Interconnects

In order to compute the power and energy-per-bit saving using ECC in the optical interconnect, we assume the Chameleon architecture [52] with 4x4 IPs (or clusters) and a system using four wavelengths per waveguide. The laser efficiency is set to $Laser_{eff} = 5\%$. Based on the model of losses, we can extract the worst case of loss for this architecture as $L_{wc} = 3.25$ dB.

4.6.1 Power and Energy-per-Bit Saving

According to Figure 4.7, at a given $BER = 10^{-9}$, the H(7,4) coding gain is 3.08 dB. The sensitivity of photo-detector at $BER = 10^{-9}$ is −17.3 dBm. The minimum laser power in dBm for a reliable communication at $BER = 10^{-9}$ without ECC is

$$PO_{Laser,U} = P_{sen}(dBm) + L_{wc}(dB) = -17.3 + 3.25 = -14.05 \quad dBm \tag{4.29}$$

or, in milliwatt,

$$PO_{Laser,U}(mW) = 10^{PO_{Laser,U}(dBm)}/10 = 0.0394 \quad mW. \tag{4.30}$$

The electrical power required for the laser for an uncoded communication is then

$$PE_{Laser,U}(mW) = \frac{PO_{Laser,C}}{Laser_{eff}} = \frac{0.021}{0.05} = 0.423 \quad mW. \tag{4.31}$$

When using Hamming(7,4), the electrical power required for the laser for a reliable

communication is

$$PE_{Laser,C}(mW) = \frac{B}{B_C}\frac{PE_{Laser,U}}{10^{ECC_{gain}/10}} = \frac{4}{7}\quad\frac{0.423}{10^{3/10}} = 0.121\quad mW \tag{4.32}$$

Furthermore, the power consumption the Hamming(7,4) encoder and decoder from Table 4.1 is

$$P_{codecs} = P_{encoder} + P_{decoder} = 0.434 \times 10^{-3}\quad mW. \tag{4.33}$$

Therefore, the **power saving using Hamming(7,4) code** is

$$\begin{aligned}\Delta P_{save} &= PE_{Laser,U} - PE_{Laser,C} - P_{codecs}\\ &= 0.423 - 0.121 - 0.434 \times 10^{-3} = 0.301\quad mW\end{aligned} \tag{4.34}$$

The energy per bit of the communication without and with using Hamming(7,4) code is

$$E_{b,U} = \frac{PE_{Laser,U}}{R} = \frac{0.423 * 10^{-3}}{4} = 105.75\quad \mu J/bit \tag{4.35}$$

$$E_{b,C} = \frac{PE_{Laser,C}}{R} = \frac{0.121 * 10^{-3}}{4} = 30.25\quad \mu J/bit, \tag{4.36}$$

respectively. The energy per bit cost per encoded and decoded information bit due to the codecs is

$$E_{b,codecs} = \frac{P_{encoder} + P_{decoder}}{R} = \frac{0.434 \times 10^{-3}}{4} = 0.1085\quad \mu J/bit \tag{4.37}$$

Finally, **the energy per bit saving** using Hamming(7,4) code is

$$\Delta E_{b,save} = E_{b,U} - E_{b,C} - E_{b,codecs} = 75.39\quad \mu J/bit \tag{4.38}$$

Figure 4.9 provides the power saving obtained by using several ECCs in Chameleon with size 4x4 IPs, $N_{wavelength} = 4$ for a laser efficiency of $Laser_{eff} = 5\%$ and a worst case of losses of $L_{wc} = 3.25$ dB. Meanwhile, Figure 4.10 provides energy-per-bit saving using the same Chameleon configuration.

As shown in Figure 4.9, RS(15,11,5) ECC provides the best performance concerning the power saving due to its highest performance in ECC coding gain. However, it also consumes the highest power in its codecs, and therefore RS(15,11,5) does not provide the

best performance in energy-per-bit saving. Then, Hamming(7,4) is the best candidate in terms of energy saving.

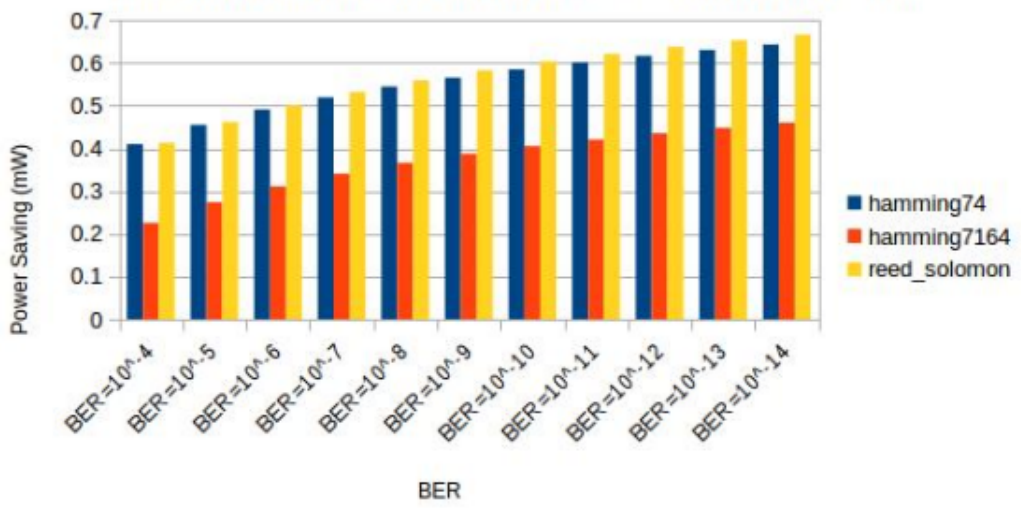


FIGURE 4.9: Power saving by using ECCs in Chameleon with size 4x4 IPs, $N_{wavelength}$ = 4. Laser efficiency is $Laser_{eff}$ = 5% and worse case of losses is L_{wc} = 3.25 dB

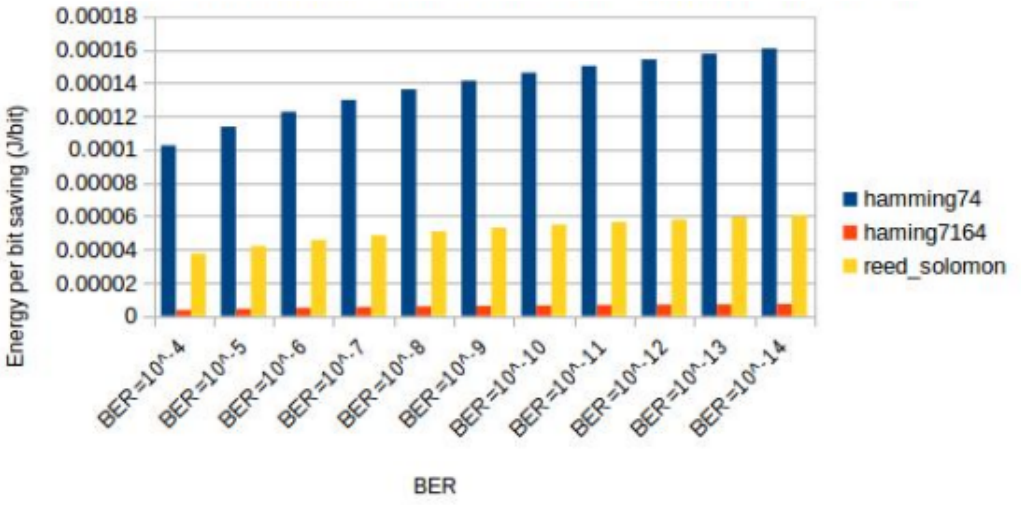


FIGURE 4.10: Energy saving by using ECCs in Chameleon with size 4x4 IPs, $N_{wavelength}$ = 4. Laser efficiency is $Laser_{eff}$ = 5% and worse case of losses is L_{wc} = 3.25 dB.

4.6.2 BER and Laser Power Trade-Offs

For on-chip light sources, we assume an integrated CMOS-compatible vertical-cavity-surface-emitting lasers (VCSEL) [94]. The temperature of the VCSEL depends on i) the optical power to be emitted (OP_{laser}) and ii) the activity of the electrical layer. Following

the methodology detailed in [57], the laser power consumption P_{laser} is estimated assuming 25% chip activity. As illustrated in Figure 4.11, P_{laser} linearly increases within the $0 - 500\mu$W optical power range but follows an exponential trend for larger values. This trend is due to the efficiency of the laser which drastically drops with high temperature.

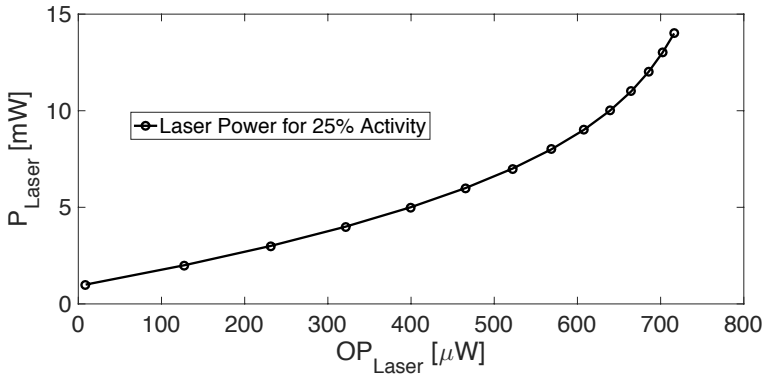


FIGURE 4.11: P_{laser} estimated from the output optical power OP_{laser} with 25% chip activity.

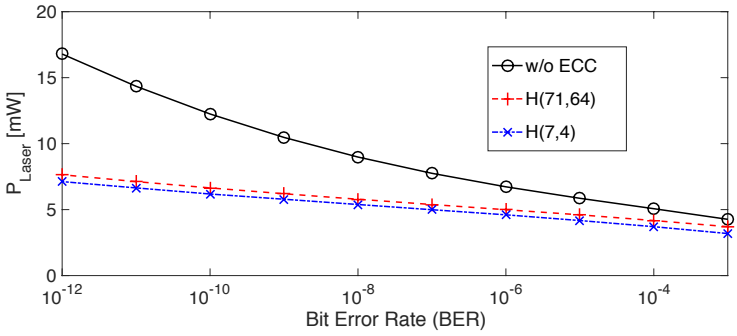


FIGURE 4.12: P_{laser} for a given MWSR channels calculated from the targeted BER and the selected ECC code.

Using the model described previously, we evaluate in Figure 4.12 the optical power signal needed to reach the targeted BER according to a given coding technique. For this purpose, we assume an MWSR architecture with 12 ONIs, 16 wavelengths, 6cm waveguide length, 0.274 dB/cm waveguide loss [18] and extinction ratio ER = 6.9 dB [87]. We assume transmissions with H(7,4), H(71,64) and without ECC, and targeted BER values range from 10^{-3} to 10^{-12}. As expected, the transmission without codes leads to a higher laser power consumption. For instance, each laser source consumes 14.3 mW for $BER = 10^{-11}$. In case H(71,64) is used, P_{laser} drops to 7.12 mW and it further decreases to 6.64 mW for H(7,4). This significant reduction in the laser power is due to the added redundancy bits, which improve the optical channel robustness. Since additional errors

in the transmission are acceptable, the optical power emitted by the light sources is reduced. Interestingly, targeting a 10^{-12} BER without ECC is not possible since it exceeds the maximum optical power deliverable by the laser (i.e. 700μW). However, reaching this BER is possible using H(71,64) and H(7,4) (P_{laser} = 7.1 mW and 7.6 mW respectively).

4.7 Conclusions

In this chapter, we investigated the use of Error Correcting Code (ECC) to reduce the laser output power according to the communication quality requirement. We have shown that using ECC not only allows reducing the laser power consumption but also allows to target BER not reachable without coding techniques and without compromising energy per bit. Since lasers significantly contribute to the optical channel power, the global power reduction of the optical interconnect is also possible under a specific scenario. This trend has been observed especially for H(71,64) ECC.

This chapter has demonstrated the advantages of using FEC on the energy efficiency of the optical interconnect based on a novel architecture [52] an some case studies of lightweight FEC with low implementation complexity and high error-correction performance for a 28 nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology.

Based on these advantages of using FEC, we present in the next chapter the optical network interface which is located between the optical and electrical interfaces. The architecture of the interface can adapt some communication requirements like communication speed and throughput. Furthermore, the optical interface manager is also presented.

Chapter 5

Optical Network Interface Design

Optical Network-on-Chip is a promising technology to leverage the interconnection bottleneck in manycore architectures. Indeed, this technology offers high bandwidth and low latency for communications between cores or clusters of cores. However, the high static power consumption of Optical NoCs (ONoCs) calls for reconfiguration of the interconnect in order to meet the performance requirements while minimizing the required energy. This section addresses this challenge and proposes a method to define, at design time, a set of ONoC execution modes to be loaded, at run-time, according to the applications' performance and energy requirements. The proposed methodology relies on an Optical Network Interfaces (ONI).

In ONoCs, the interface between the optical and electrical domains has an essential role on overall system performance. Indeed, even if the optical components show interesting performance, the associated digital architectures must satisfy some characteristics to not limit the communication medium. This interface is called Optical Network Interface (ONI). For instance, the operating frequency of both domains are not similar and the throughput must be adapted. Moreover, the way an ONI is designed also provides more or less flexibility to use the ONoC, like an adaptive number of wavelengths for each communication or tuning the power of the laser.

In this chapter, we propose an ONI architecture providing high flexibility: the data of a core can be associated to any number of wavelenghts, using or not ECC. Moreover the power of the laser can be tuned by acting on the laser driver. Finally we propose a high

level shared component called ONoC Configuration Sequencer (OCS) allowing for the sources and destinations ONIs to be configured at run time.

5.1 Introduction

Multiprocessor System-on-Chip (MPSoC) are evolving towards the integration of hundreds of cores on a single chip. Designing an efficient interconnect for such complex architectures is challenging due to the ever growing data exchange between processors. Networks on Chip (NoCs) have been proposed to overcome these issues but they are now reaching their performance limits. Indeed, packetization and depacketization of data drastically impact NoC latency [77] and the same bandwidth for all router ports is usually assumed whereas processor bandwidth requirements vary significantly [16]. NoC efficiency thus needs to be further improved in order to interconnect systems with ever increasing number of cores and required bandwidth density efficiently [4].

To overcome the limitations of classical NoCs, nanophotonic interconnects are a promising technology to support communications in MPSoCs. Indeed, Wavelength Division Multiplexing (WDM) allows for the propagation of multiple signals simultaneously on a same waveguide [1], thus leading to high aggregated bandwidth. However, WDM also leads to inter-channel crosstalk noise [49], which negatively impacts the Signal to Noise Ratio (SNR) and, therefore, the Bit Error Rate (BER). The BER to be reached depends on the application requirements and is closely related to the optical devices characteristics, since it depends on the photodetector sensitivity [27], on the Microring Resonator transmission spectrum, and on the optical signal power emitted by the laser sources. The higher the number of signals propagating simultaneously, the higher the crosstalk and the higher the laser output power needed. This thus leads to the following conflicting objectives: high performance communications tend to rely on an exhaustive use of the available wavelengths while energy efficient communications involve a parsimonious use of signals which occupy distinct and separate wavelengths. Using an Optical NoC (ONoC) to support the communications of a given application is thus a tedious task, especially if performance, power and BER objectives are likely to evolve with the execution context.

Hence, for an application executed on a given architecture, several solutions allow implementing the communications, each one providing an optimal solution but with a unique

trade-off between energy and performance. In the state of the art, ONoCs can be classified into two families regarding the communication allocation strategy: online or offline. However, to the best of our knowledge, there is no architecture allowing run-time adaptation of the ONoC to meet energy and performance application requirements for both types of allocations.

To allow run-time adaptation of the ONoC according to energy and performance requirements of the executed applications, a method has been proposed by J. Luo *et al.* in [65]. The method relies on an offline framework to generate a set of ONoC configurations to be stored in a particular ONIs that we propose in this chapter. This ONI works in conjunction with an ONoC configuration sequencer located in the center of the optical layer (Figure 5.1), that we also propose in this chapter. The ONI then selects at run-time the configuration to be loaded according to the application needs.

5.2 Run-time Adaptation of ONoC Energy and Performance

5.2.1 Considered Architecture and Applications

We consider a 3D ONoC, i.e., a 3D integrated circuit supporting mixed-technology with an electrically controlled Optical NoC. It combines the benefits of silicon photonics and 3D stacking to overcome traditional electrical network limitations. Photonic interconnect delivers high on-chip bandwidth and low latency while 3D stacking can reduce the interconnect distance. Figure 5.1 shows a ring-based 3D ONoC architecture composed of two layers interconnected by TSV: i) on the bottom, an electrical layer implementing processing cores and ii) on the top, an optical layer with optical routers and waveguides. Following the layout defined in [113], a centralized ONoC configuration sequencer driven by an Operating System allows run-time adaptation of the ONIs, as illustrated in red in Figure 5.1. The OS is responsible for deploying tasks among the cores and defining the strategy to adapt the ONoC to meet application requirements, such as energy consumption or execution time (called performance within this paper). The sequencer is responsible for reconfiguring the ONoC according to the mode selected by the OS.

Figure 5.2 illustrates the dependencies between the application tasks, the allocated bandwidth and the performance. Applications are represented as a Directed Acyclic Graph

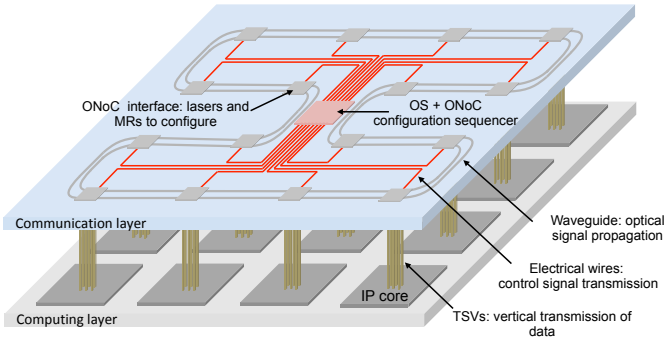


FIGURE 5.1: Considered 3D ONoC architecture with the configuration sequencer located in the center of optical layer.

(DAG) as depicted in Figure 5.2.a, where each vertex t_i represents a task and each directed edge ($c_{i\to j}$) represents a communication from t_i to t_j. In this example, we assume that tasks t_0, t_1, and t_2 are mapped onto different processors. Communications $c_{0\to1}$, $c_{0\to2}$, and $c_{1\to2}$ are implemented using an ONoC which is configured according to execution performance and energy requirements.

As we consider WDM communication and laser power tuning, the energy consumption and the execution time of the application are linked to the resources allocated for each communication of the DAG. Indeed, it is possible to adapt the bandwidth for each communication, by varying the number of wavelengths, and to adapt the power laser to meet a targeted communication quality through the BER (not illustrated in this figure). Figure 5.2.b illustrates energy versus execution time plot and shows a Pareto front of communication solutions for the architecture. This figure also highlights HP (High Performance) and LP (Low Power) modes on the Pareto front, which either tries to maximize performance or minimize energy or power consumption.

Figures 5.2.c and 5.2.d are the communication graphs obtained considering i) the mapping on the processors and ii) the bandwidth allocated to each communication. While a complete communication task would consider all possible communication end-time sequence scenarios (for instance, $c_{1\to2}$ can terminate before or after $c_{1\to3}$), we consider a reduced graph for which communication times are estimated. It is worth mentioning that a reduced graph improves the scalability of our approach by simplifying the design of the controller and by reducing the memory footprint. Following the method detailed in Section 5.3.1, each state of the communication graph is associated to a configuration Q.

Figures 5.2.e and 5.2.f show the execution traces of the HP and LP solutions. We can

clearly see that the HP solution reduces the execution time of the DAG by using more bandwidth for each communication compared to the LP solution.

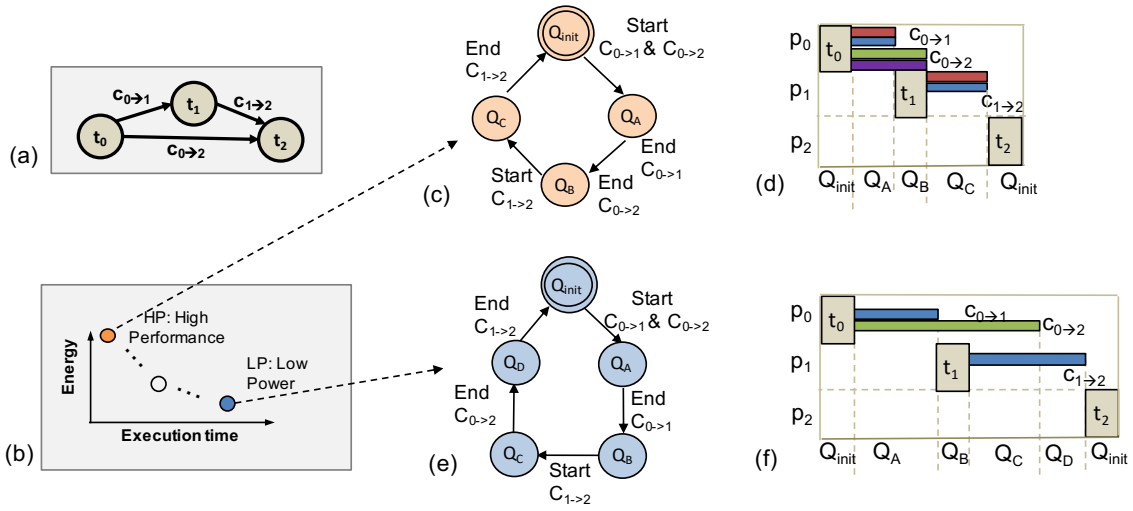


FIGURE 5.2: Energy-performance trade-off: a) Application represented as a DAG, b) Energy versus Performance plot highlighting High Performance (HP) and Low Power (LP) modes, c-d) ONoC configuration sequence for HP mode and the resulting execution traces, e-f) ONoC configuration sequence of LP mode and the resulting traces.

5.2.2 Architecture of the Sequencer

The proposed approach requires two hardware blocks, as depicted in Figure 5.3: i) an ONI manager, located in each ONI, in charge of activating the Lasers and MR, and ii) an ONoC configuration sequencer, shared among all the ONIs, in charge of sequencing the configurations of the ONIs.

An Optical Network Interface, ONI (illustrated on the right part of Figure 5.3), integrates a receiver Rx and a transmitter Tx. The transmitter is composed of on-chip laser sources that can emit and inject optical signal at a specific wavelength into the waveguide. The power generated by the Lasers can be configured. In this example the Lasers can be configured independently among four levels of power. The data are directly transmitted from these lasers through current modulation (OOK) and each laser source can also be turned OFF for energy saving. As the lasers are sending data in serial and as a core sends data in parallel on N_{bits}, a WDM stream serialization is required in order to perform the serialization and allocation of the serial data to the selected wavelengths (i.e. lasers). The receiver part includes wavelength-specific MR that can be turned ON

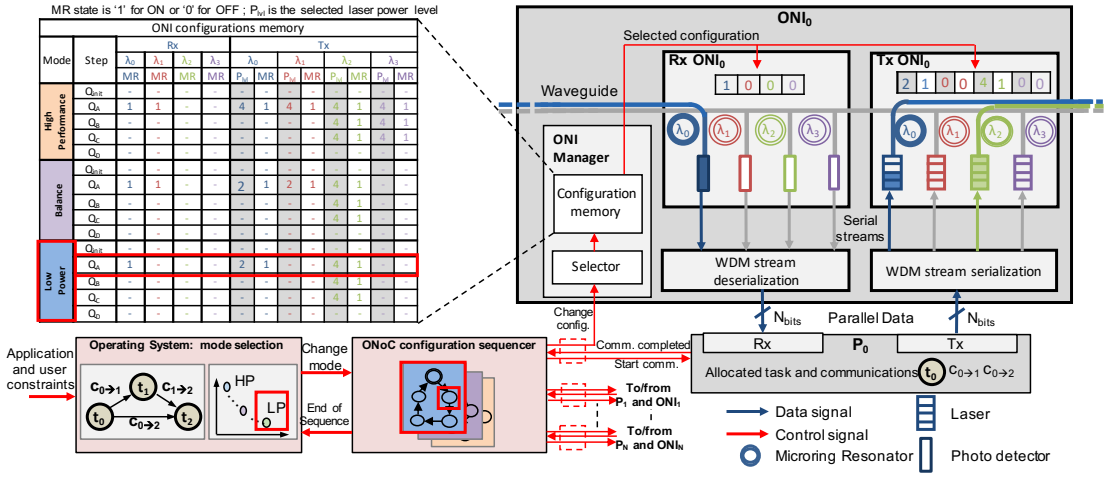


FIGURE 5.3: Proposed Optical Network Interface architecture.

or OFF to configure respectively drop or pass-through operations of the signals at a given wavelength. Signal dropped from a waveguide reaches a photodetector, where opto-electric data conversion generates an electrical signal suitable for the electronics part of the receiver. The considered architecture allows the reuse of wavelengths to realize multiple independent communications in a single waveguide. The receiver includes a WDM stream deserialization to perform serial to parallel conversion on the received data. Each ONI includes an ONI Manager in charge of configuring the receiver and the transmitter. It includes an ONI configuration memory which stores the configurations to apply on the MRs and Lasers for different operating modes and at different steps composing a sequence of configurations.

As mentioned above, the second hardware block required is the ONoC configuration sequencer in charge of synchronizing all the ONI Managers of the ONoC. It includes a state machine explained in Section 5.3.2 as a sequence diagram. This block takes as input decision from the Operating System in order to select the configuration mode satisfying application requirements. Moreover, it is connected to the ONIs through three signals. The first is a one-bit signal indicating the ONI to start exploiting the configuration associated to the current Step and Mode selected in the ONI configuration memory. The second is also a one-bit signal generated by the ONIs indicating that a step is over. The last signal bit-width depends on the number of Modes embedded in the ONI configuration memory and allows to select the mode to apply.

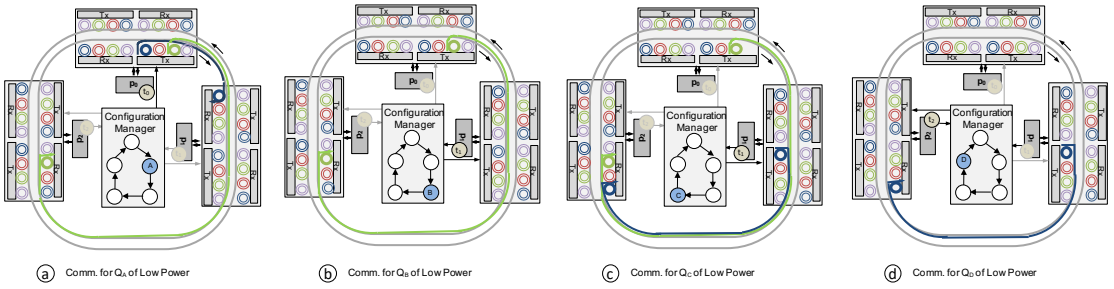


FIGURE 5.4: Illustration of the run-time management of energy-performance trade-off: example of ONoC ONI's configuration evolution in LP Mode

5.2.3 Run-Time Management of Energy-Performance Trade-off

Figure 5.4 illustrates the configuration of the ONIs for each step of the configuration sequence in the Low Power mode. In this mode, p_0 sends a control signal to the configuration manager when t_0 execution ends and when data involved in $c_{0\to1}$ and $c_{0\to2}$ are ready for transfer. The manager switches from configuration Q_{init} to Q_A: Tx_0 and Rx_1 are reconfigured with the values stored in the configuration memory. Two on-chip lasers are powered on to emit optical signals for purpose of reducing energy consumption (the laser output powers are not illustrated for the sake of clarity) as shown in Figure 5.4.a. For low-latency purpose, the ONoC is reconfigured in parallel, which is implemented using dedicated electrical wires connecting the controller to the optical devices. Once the new configuration is loaded, the data transfer starts and, once it ends, another control signal is sent to the configuration manager to disable the communication channels. For this purpose, a new configuration (Q_B as shown in Figure 5.4.b is loaded i.e. the lasers and the MR involved (blue one) in the communication are turned OFF. Figure 5.4.c illustrates communication $c1 \to 2$ carried out by the controller. The reconfiguration of the interfaces to implement a new communication has no impact on the ongoing communications: in this example, green signal on p_0 to p_2 waveguide segment is used for $c_{0\to2}$ while $c_{1\to2}$ is carried out using blue wavelength (reconfiguration $Q_B \to Q_C$). Then $c_{0\to2}$ ends and the green laser and MR are turned off as illustrated in Figure 5.4.d (Q_D). Finally, the resources are released and become available for the next iteration.

5.3 ONoC Configuration Sequencer

5.3.1 Generation of Configuration

We consider the use of the framework presented in [62] to generate the ONoC configuration sequences. This flow takes as inputs an application mapped onto the 3D architecture illustrated in Figure 5.1. The application is modeled as a task graph characterized by task execution times, amount of data transmitted between tasks, and minimum BER to be reached. The design flow relies on device parameters since they impact the performance of optical communications. Instance of parameters are photodetectors sensitivity, waveguide losses and MR model. Regarding the laser, we take the data-rate, the efficiency, the maximum output power, and the number of power levels available into account. The aim of the flow is to optimize both power consumption and application execution time. For this purpose, our framework explores both device-level and system-level parameters. Based on a set of device and system input parameters, a multi-objective optimization is carried out using a genetic algorithm due to the two contradictory objectives. In the genetic algorithm, the ONoC configuration modes are represented by chromosomes and the genes encode both wavelength allocations and laser power levels. Finally the resulting ONoC configuration modes on a Pareto front from the multi-objectives optimization are thus reported, including low-power solutions, which tends to minimize the number of used wavelengths, and high-performance solutions, for which multiple wavelengths are allocated to shorten the communication time. It has to be noticed that the framework also optimized the selection of the wavelengths in order to reduce the crosstalk. Then the obtained trade-off configuration modes could be embedded in the system and be loaded on run-time according to the execution context (e.g. high performance and low power) which is out of the scope of this paper. Refer to [62] for more details on the generation of solutions.

Figure 5.5 illustrates individual coding and the corresponding ONoC configuration and how we generate the communication configuration that are embedded in each ONI. As depicted in Figure 5.5.a, we assume three interfaces, four wavelengths (i.e. four lasers per interface) and four laser output power levels. Tasks t_0, t_1 and t_2 are mapped on processor p_0, p_1, and p_2, respectively, which leads to optical communications between p_0 and p_1 ($c_{0\to1}$), p_0 and p_2 ($c_{0\to2}$), p_1 and p_2 ($c_{1\to2}$). The chromosome is divided into as many parts

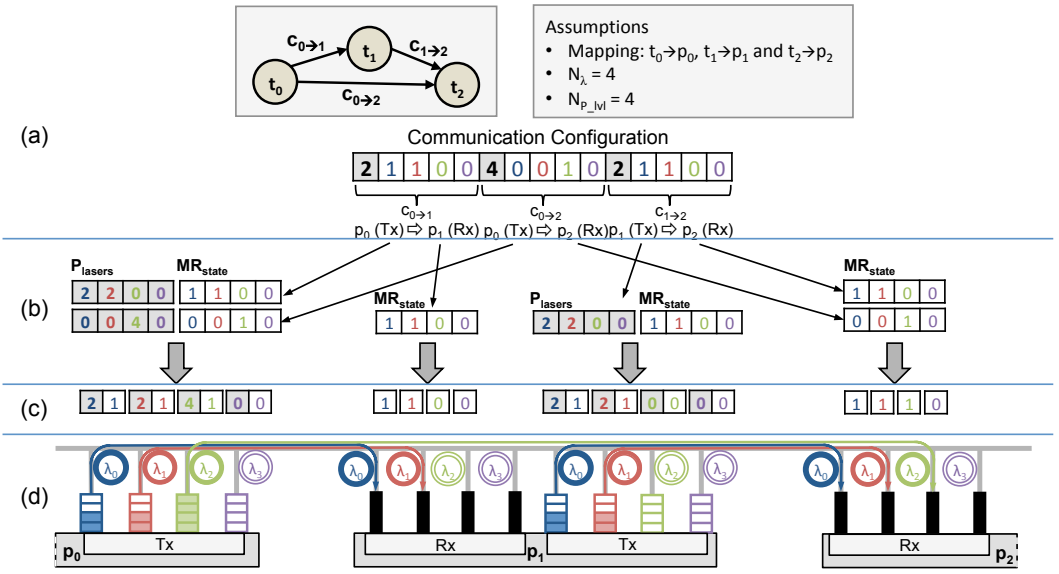


FIGURE 5.5: Generation of the configurations: a) DAG description, architectural assumptions and the results of the offline optimization framework, b) Extraction of each ONI configuration, c) Result of the ONI configurations, d) Configuration of each ONI with respect to the extraction configurations.

as there are communications (three in the example) [62]. Figure 5.5.a shows one of the solution given by the framework. It is represented as a chromosome given the bandwidth and power allocation for each communication. The first gene of each chromosome part gives the selected laser output power level; it is an integer value corresponding to the laser configuration. The following genes correspond to the wavelengths utilization: value 0 or 1 indicates that a wavelength is used or unused, respectively. In the example, both $c_{0\to1}$ and $c_{1\to2}$ use λ_0 and λ_1 while $c_{0\to2}$ is implemented using only λ_2. Obviously, the more wavelengths are allocated for a given communication, the higher the bandwidth.

The configuration of each interface is obtained as follows and is illustrated in Figure 5.5.b. MR state and Laser power levels are extracted from the chromosome for each Tx and Rx of the ONIs. As we can see in this example, the Tx of p_0 will handle two communications that use different wavelengths and power levels. Then, the configurations are merged and the results configuration of each Tx and Rx are obtained, as shown in 5.5.c.

Finally the configuration can be applied to the ONIs as illustrated in 5.5.d. First, optical channels are open by switching ON the MRs involved in communications (i.e. MRs localized in the transmitter Tx of the source processor and the receiver Rx of the destination). Then, the power of the optical signals propagating through the channels is defined according to the selected lasers power level. In the example, at the transmitter

of p_0 interface, three MRs are turned ON to implement communications $c_{0\to1}$ (λ_0 and λ_1) and $c_{0\to2}$ (λ_2). On the receiver side, the MRs corresponding to λ_0 and λ_1 are set to the ON state in p_1 interface, while the MR corresponding to λ_1 remains OFF to let the signal reaching p_2 interface were it will be dropped. In the chromosome part dedicated to $c_{0\to1}$, the laser output power level is set to 2: in p_0 interface, the lasers emitting at wavelength λ_0 and λ_1 are set to 50% of the maximum power. In the same interface, laser at λ_2 is set to 100% to match value 4 in corresponding gene for $c_{0\to2}$.

5.3.2 ONoC Sequencing Illustration

Figure 5.6 illustrates the relation between the Operating System (OS), the ONoC configuration Sequence, and the ONIs. Regarding the communication through the ONoC, the OS is only in charge of defining the mode (energy-performance trade-off) of the communication. It is possible to change the mode at the beginning of a new sequence. Regarding the sequencing of steps within a sequence, the ONoC configuration sequencer sends the order to apply the ONI configuration for Tx Rx by using a one-bit signal to the ONI manager. The ONI Manager reads the associated memory containing the Tx and Rx configurations, hence the communication can start.

When the communications are over for a processor, or when no communication are necessary in a step, the ONI manager associated to a core sends back a one-bit signal to the ONoC configuration sequencer. When all the communications are completed, the ONoC configuration sequencer indicates to all the ONI to go through the next step. Hence, the aforementioned sequencing is repeated.

5.4 Performance Results

In this section we show the energy versus performance trade-offs available in an ONoC. We consider the architecture in Figure 5.1 in which each ONI is connected to a cluster of four electrically connected cores. We assume two waveguides, eight wavelengths per waveguide, five configurable levels of electrical power for the Lasers: 2, 4, 6, 8, and 10 mW. Table 5.1 summarizes the technological parameters used to generate the ONoC configurations with the framework proposed in [62]. Regarding the applications, we use a random task graph generator that provides applications including from 52 to 107 tasks

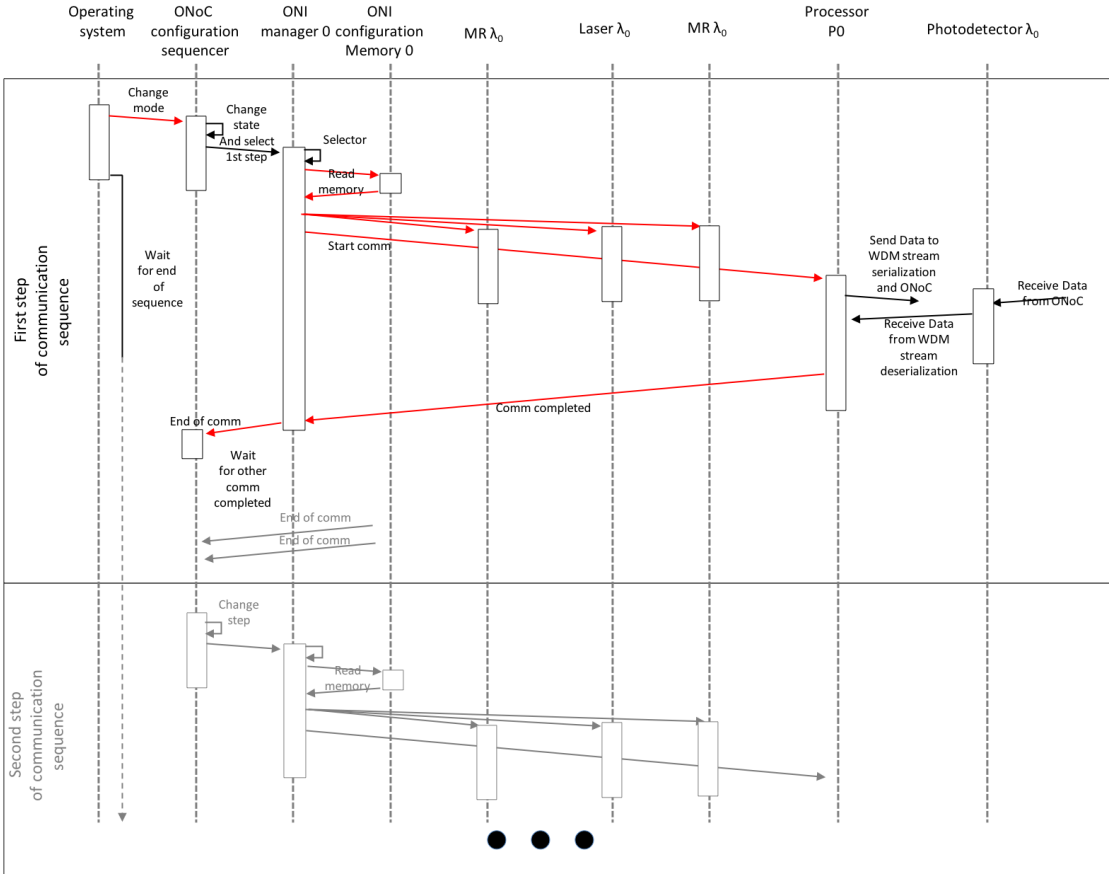


FIGURE 5.6: Sequence diagram detailing the interactions between the Operating System, the ONoC configuration sequencer, and the ONIs.

and from 80 to 158 communications. The task execution time values are randomly selected between [100, 1000] clock cycles (cc) and the communication volumes are randomly selected within [100, 1000] bytes. The targeted BER is 10^{-9} and each task is randomly mapped on a dedicated core. As we assume shared memory within a same cluster, no latency is assumed for intra-cluster communications.

Table 5.2 summarizes the characteristics of the task graphs and the total energy and execution time in clock cycles (cc) required. Since the generation of the ONoC configuration leads to a Pareto front with several solutions, we only show the solutions with i) the lowest energy consumption (denoted Low Power in the table) and i) the lowest execution time (High Perf.). As shown in Table 5.2, the solutions offer, on average, 44% energy variation and 71% execution time variation trade-offs. From these solutions, the designers can implement in the configuration memory of the ONI manager several solutions that provide intermediate trade-offs. These results demonstrate the efficiency of flexible wavelengths allocation and laser output power tuning to adapt the nanophotonic

interconnects according to application requirements.

Parameter	Value	Ref
Waveguide propagation loss	-0.274 dB/cm	[19]
Photodetector sensitivity	-20 dBm	[42]
Laser efficiency	15%	[42]
$\Delta\lambda$	0.4 nm	[3]
FSR	8 nm	[3]
$-3dB$ MR bandwidth	0.26 nm	[3]

TABLE 5.1: Technological parameters.

Graph ID	**Number of Tasks/Comms**	**Energy (nj)**			**Execution Time (kcc)**		
		Low Power	**High Perf.**	**Variation**	**Low Power**	**High Perf.**	**Variation**
TG 1	55/80	141	187	1.33	41.2	23.8	1.73
TG 2	52/78	118	194	1.64	37.9	23.6	1.62
TG 3	57/82	102	120	1.18	39.9	24.6	1.84
TG 4	60/92	141	195	1.38	37.3	22.8	1.62
TG 5	63/93	128	193	1.51	41.2	24.6	1.89
TG 6	62/92	147	236	1.61	43.2	24.4	1.75
TG 7	56/87	103	148	1.44	31.7	19.9	1.57
TG 8	63/91	112	156	1.39	37.5	23.3	1.60
Average		**124**	**179**	**1.44**	**38.7**	**22.7**	**1.71**

TABLE 5.2: Energy-performance trade-off variation possibilities.

5.5 Design of the ONI and OCS

As it was already shown, to allow run-time dynamicity in the ONoC performance, the ONoC must integrate specifics blocks, like the OCS and the ONIs. In this section, we present the different proposed blocks required to apply the aforementioned methods.

5.5.1 Transmitters and Receivers for WDM in ONIs

5.5.1.1 Operating Principle

Figure 5.7 illustrates that the ONI is located between optical and electrical domains, each domain having different signal frequency for receiver and transmitter. For example, a modulation frequency F_{mod} set to 10GHz provides a throughput of 10Gbit/s on 1-bit serial data transmission. According to [2], this is the optical bandwidth to obtain good trade-off between throughput and energy efficiency of each separated wavelength.

Whereas, in the electrical domain, IPs would rather communicate at a much lower frequency, noted F_{IP}, e.g. 1GHz, but with parallel data bus of N_{data} width, such as 64 bits.

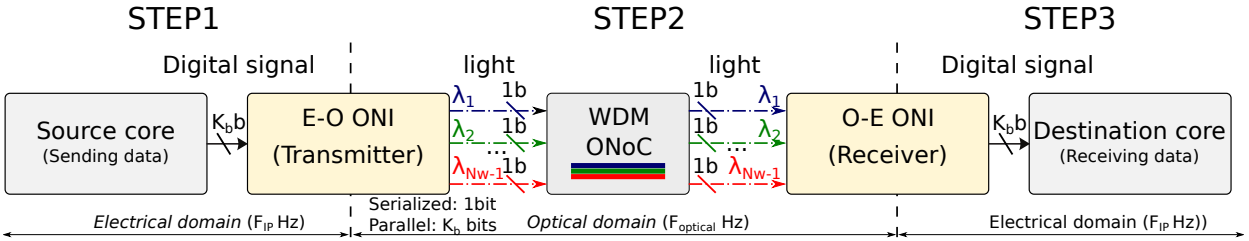


FIGURE 5.7: Illustration of the different clock domains for the electrical and optical domains

Figure 5.8 illustrates the architecture of the transmitter and receiver interfaces in the case of three modes (uncoded and two Hamming code configurations). The energy/performance management system selects the coding technique according to communication requirements (e.g. task priority, BER). In addition to the mode with direct modulation (uncoded transmission), different coded modes (corresponding to different Hamming encoder configurations in the figure) can be selected. The encoded data are outputted to a serializer in order to generate the stream of serial data at the required F_{mod} speed. The operated clock of the serializer register equals the modulation speed. In this chapter, we did not investigate data flow control and multiple-wavelength allocation, which have already been effectively addressed in [108] and [76], respectively.

In order to understand the operation principle of the interface, we take an example of the architecture which has been presented previously with Hamming codes. Other cases are shown in the rest of this chapter (see Section 5.5.2). Figure 5.8 illustrates the architecture of ONI based on the Hamming codes with different size of data input. The management part allows the system to control the related components of the interface: i) the configurations of encoders, (ii) the serialisation in one or several serial streams, and iii) the allocation of wavelengths for these data serial flows. In Figure 5.8, this control is represented by the enable input of each block. The initiator of the communication is a task application, shown in Figure 5.8 for task T_3 in the bottom left. The requirement of this task is captured by the energy/performance management system that has a precise knowledge of the number of wavelengths and which wavelength takes part in the communication. From this global information, the system evaluates the number of wavelengths that can be allocated for the communication initiated by task T_3. We assume

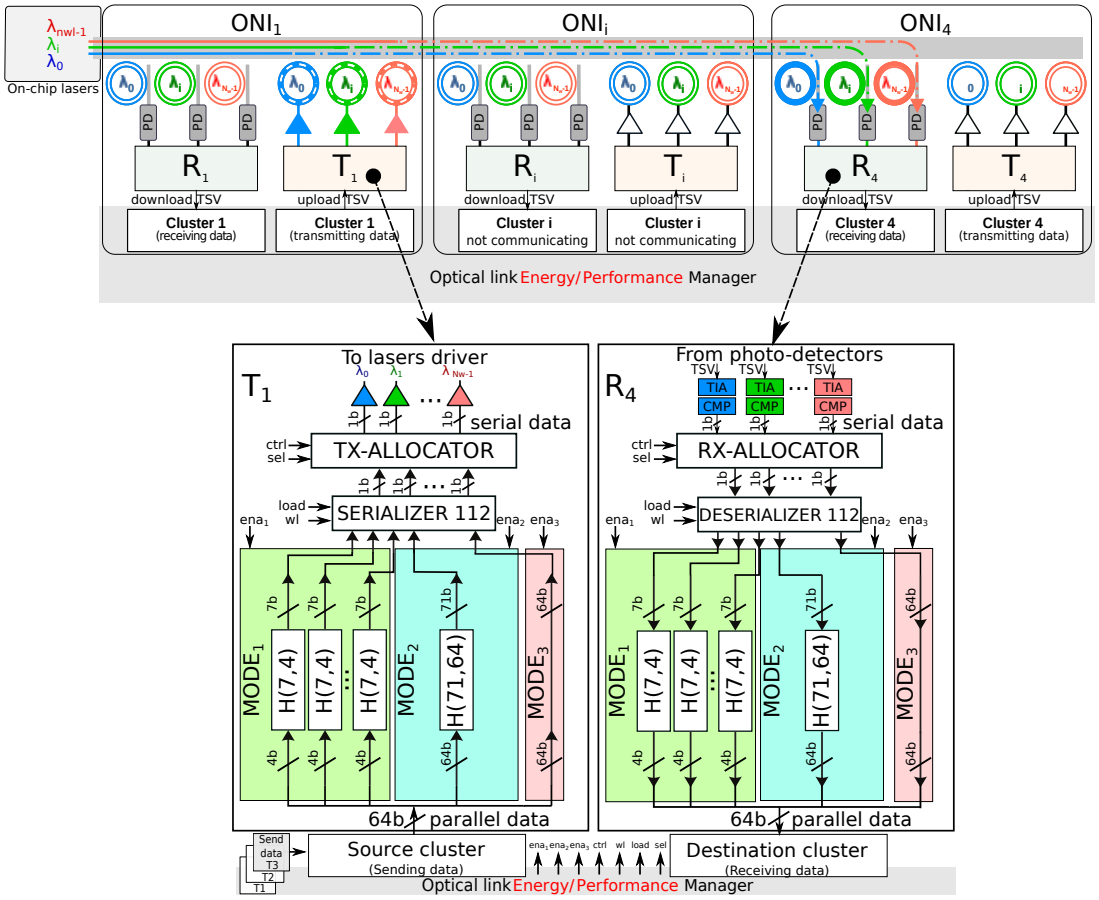


FIGURE 5.8: Architecture of the optical network interface using Hamming code with three communication strategies

here that the allocation system decided to allocate three wavelengths (λ_0 blue, λ_i green and $\lambda_{N_{WL}-1}$ red) for this communication.

In Figure 5.8, we assume that the allocation decides for the encoding of data by H(7,4) encoder. Then the encoding requires 16 H(7,4) encoders in parallel to encode 64-bit data. This encoding led to the addition of redundancy bits, 3 bits of redundancy for 4 bits of data, leading to the addition of 48 bits to encode a 64-bit bus. Therefore, the output of the encoding is a 112-bit codeword that is sent to the serializer. The allocation of three wavelengths for communication leads to dividing the flow of 112-bit codewords into three serial streams. Finally, three serial streams are used in order to modulate selected lasers and to switch on the micro-resonators to inject the wavelengths in the waveguide.

At the receiver side, a symmetrical structure is implemented. According to the allocated wavelength, the control system can configure the ONI receiver by activating i) the corresponding micro-resonators for ejecting the wavelengths, ii) the deserialization of the

binary data streams to restore the information bits from the 112-bit codeword, and iii) the decoder to receive the data bits.

The interfaces with the proposed three possible communication modes (H(7,4), H(71,64), and uncoded) have been synthesized using 28nm FDSOI technology library using Synopsys Design Vision. The interfaces have been designed for 64-bit data width (N_{data} = 64) to operate at F_{IP} = 1 GHz and allowing to reach F_{mod} of 10 Gbps. The synthesis results are presented in Table 5.3 page 91. In this table, in order to encode the 64-bit data, the interface requires 16 parallel H(7,4) coders and decoders, whereas only one H(71,64) codec is required. The Hamming blocks are clocked at F_{IP} and compute the result in one clock cycle. The Serializer and Deserializer are operated at F_{mod} = $10Gbps$. In the following section, we introduce the details of the ONI transmitter (Electrical – Optical Interface) with its corresponding blocks.

5.5.1.2 Design of the Electrical – Optical Interface

Serializer Figure 5.9 presents the structure of the data serializer block. The serializer in this figure can be able to support the allocation with 1, 2, 4, 8 wavelengths respectively. According to the communication requirements, the number of allocated wavelength can be extended by using more shift registers with similar architecture. The specific feature of this block is that each communication could be implemented by one or several wavelengths to improve the communication time and increase the bandwidth through Wavelength Division Multiplexing (WDM) scheme. In general, the serializer could be configured to produce N_λ wavelengths. In this case, the serializer must be able to generate multiple streams of data serial outputs which are operated in parallel.

Transmission Allocator In order to limit the crosstalk between the signals which has the very closed wavelengths, the signal is allocated by the allocation part before coming to the driver circuit of the laser sources which operate at $F_{optical}$ = 10 GHz [2]. This feature is presented in Figure 5.10. The block has N_{max} MUX $(N_{WL}, 1)$, N_{WL} inputs and N_{max} outputs. The inputs are connected directly to the output of SERIALIZER block, the outputs are connected to the laser driver circuit for a given wavelength. By controlling the select input pin of each MUX $(N_{WL}, 1)$, the output is connected to the corresponding input. In order to avoid the crosstalk, in this block, the number of outputs is greater than

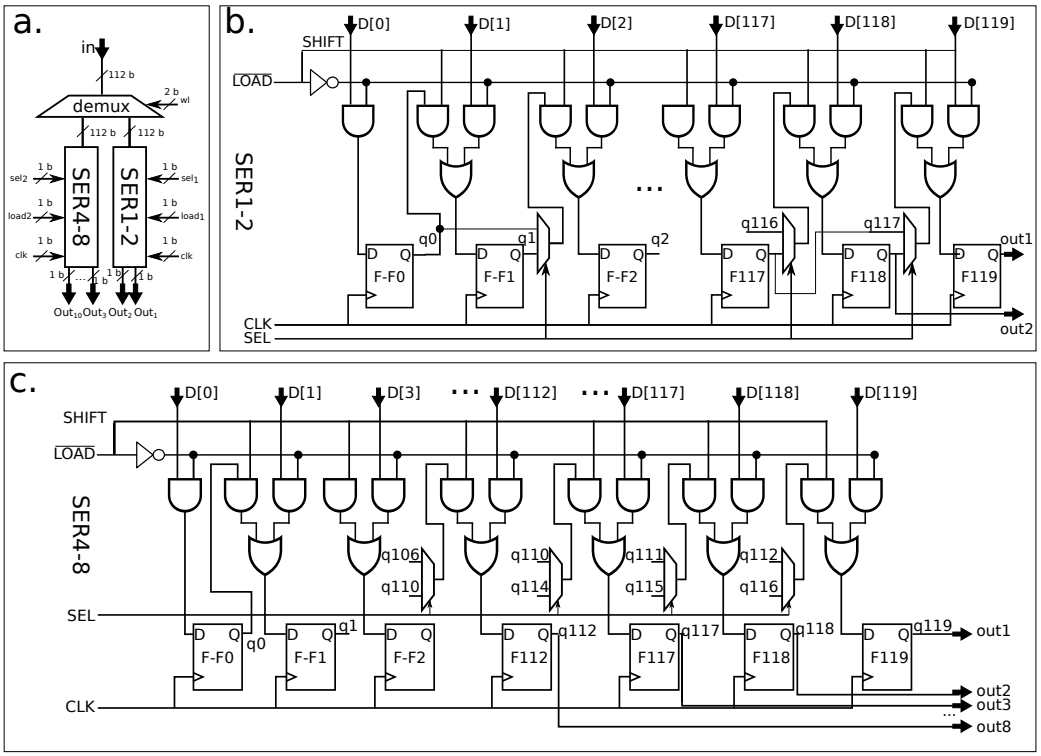


FIGURE 5.9: **a)** Overall structure of the data SERIALIZER **b)** Shift register with 1 and 2 outputs, respectively **c)** Shift register with 4 and 8 outputs, respectively

the number of inputs. Hence there are some unnecessary outputs which are turned off by the C_0 to $C_{N_{max}-1}$ input signal. This signal is controlled by the energy/performance management unit which is located in the electrical layer of the ONoC.

The modulated signal is transferred in the waveguide of ONoC until reaching the photodetector where the lightwave signal is converted into electrical current. This signal then passes through the trans-impedance amplifier (TIA) and comparator (CMP) circuit [84], [28]. Finally, the signal is recovered in the receiver interface which is presented in the following section.

Receiver Similarly, the design of the receiver interface is presented in Figure 5.8. The receiver is composed of the micro-ring resonator which can be turned ON or turned OFF in order to drop or pass through the optical signal. The optical signal injected in the wave-guide propagates until reaching the photo-detector which converts the optical signal into electrical signal. A parallel link transmits several serial streams of transformed data into the receiver-allocator. The architecture of this block is similar to the transmitter-allocator. Figure 5.12 presents the architecture of the receiver-allocator in which the number of input N_{max} is greater than the number of outputs. The energy/performance

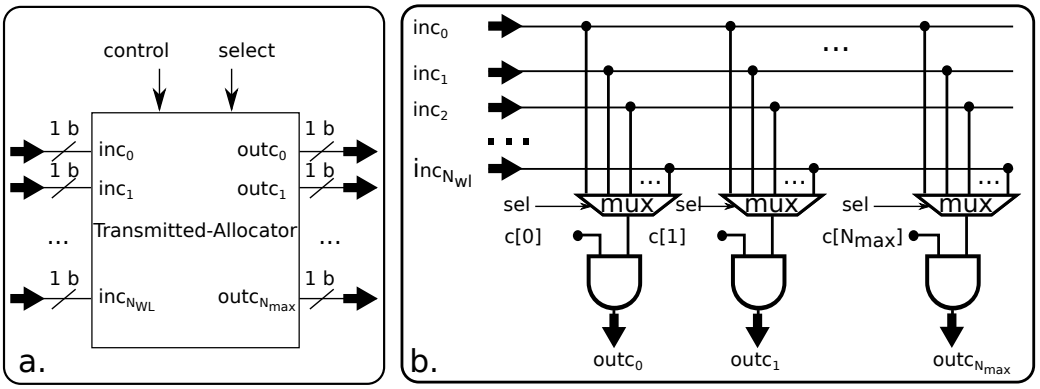


FIGURE 5.10: a. Overview of the transmission allocator b. Corresponding detailed structure

management unit also controls the control signal due to the allocation protocol. The allocated signal is then loaded into the deserializer block which operates at F_{mod} = 10 GHz.

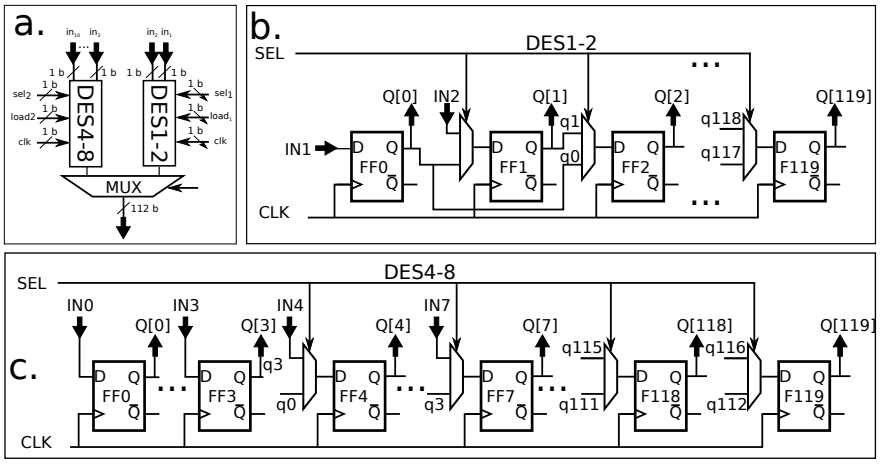


FIGURE 5.11: **a)** Overall structure of the data DESERIALIZER **b)** Shift register with 1 and 2 inputs, respectively **c)** Shift register with 4 and 8 inputs, respectively

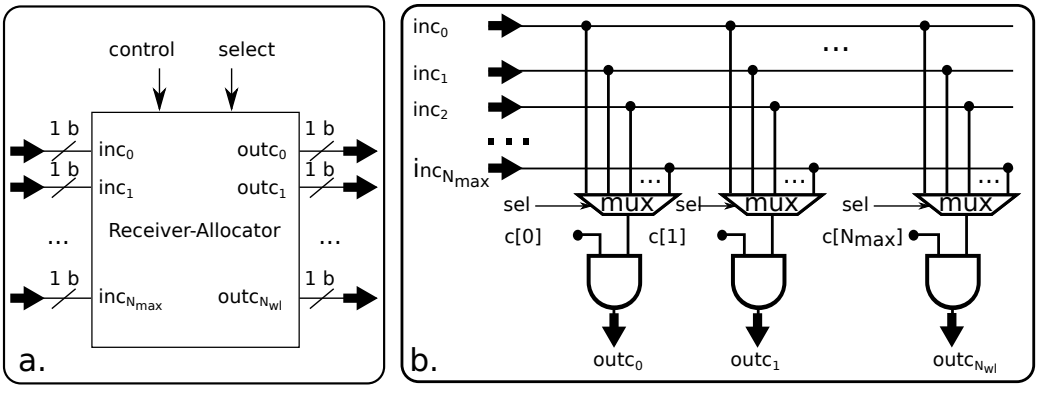


FIGURE 5.12: Receiver allocator crossbar

The deserializer block showed in Figure 5.11 converts the data from serial to parallel. Due

to the frequency of the optical domain, this deserializer also operates at the frequency of $F_{optical}$ = 10 GHz. The deserializer can support the allocation with a maximum of 8 wavelengths. However, in the general case, the design can be easily extended to produce N_λ wavelengths. Similarly to the encoders, the decoder is also composed of several decoders operating in parallel. The type and the size of the decoder must be the same with correspond encoder to adapt the bandwidth condition of the communication. For instance, if the encoder uses the Hamming encoder, the receiver must use the same type with the same size as the Hamming decoder.

5.5.2 Results and Evaluation of WDM Stream Serialization and Deserialization Interface

Evaluation Methodology Our methodology to evaluate the energy, area and execution time of the proposed interface is based on different simulations and synthesis tools: Mentor Graphics Modelsim, Synopsys Design Compiler and Synopsys Primetime. There are three corresponding steps to estimate the performance of the interface. Firstly, each element of the interface is designed in Verilog and then validated at the RTL level with Modelsim. Secondly, the different blocks of the interface are implemented at gate level using a 28 nm FDSOI technology. Area and timing results are obtained from Design Compiler. Finally, the power estimation is obtained by creating a back annotation of the switching information which is provided by the VCD file generated during gate-level simulation in the second step. The following section presents more details about the synthesis results of the interface with both the Reed-Solomon and Hamming codes.

Synthesis Results In this section, we present the synthesis results of the interface in which two case studies of FEC are included: Hamming codes and Reed-Solomon codes. Table 5.3 shows the synthesis results of the interface with the area, timing, and power reports. The interface has been designed for 64-bit data, and the operating frequency in the IP domain F_{IP} is 1 GHz. According to the previous chapter, there are two modes of communication: with Hamming code (Hamming (7,4) or uncoded). As we can see in Table 5.3, to encode the 64-bit data, the interface needs 16 parallel Hamming (7,4) encoders/decoders. These FEC codecs operate at F_{IP} frequency, and they take one clock cycle to compute the result. In order to select the coding technique which takes part in the

communication, these Hamming codes are selected by the MUX and DEMUX blocks. The encoded data are serialized by serializer block at F_{mod} frequency to modulate the laser source. This serializer is a well-known architecture based on shift-registers, with a depth equal to the input size. These registers can be loaded with the input data by the use of a two-bit MUX located in each register input. Regarding the deserializer, its architecture is also based on shift-registers with a depth equal to the output size. These straightforward solutions allow achieving a high throughput required by the optical modulation speeds while limiting the area. Table 5.3 also shows the critical path of this block is 70 ps. It means this block can operate at 10 GHz frequency to meet the transmission condition speed of the optical domain (10 Gbps).

The total area cost of the transmitter and receiver interfaces is $2795\mu m^2$ and $2493\mu m^2$, respectively. The static power is low with $28.4\mu W$ and $17.2\mu W$ respectively thanks to the 28 nm low-leakage technology.

TABLE 5.3: Synthesis results of the proposed ONI using Hamming (7,4) codes

TX	Amount	Critical Path (ns)	Total Area (μm^2)	Static Power (μW)	Dynamic Power (mW)	Total Power (mW)
H(7,4) Enc	16	0.21	551.04	1.76	3.13	3.14
DEMUX	1	0.03	762	10.69	1.45	1.46
Serializer	1	0.09	1664	25.80	1.2	1.23
TX Allocator	1	0.09	90.10	0.843	0.072	0.073
RX	**Amount**	**Critical Path (ns)**	**Total Area (μm^2)**	**Static Power (μW)**	**Dynamic Power (mW)**	**Total Power (mW)**
H(7,4) Dec	16	0.3	783.36	2.53	3.80	3.81
MUX	1	0.8	676	10.8	1.55	1.56
Deserializer	1	0.07	966.5	13.6	1.03	1.04
RX Allocator	1	0.09	95.3	1.07	0.171	0.172

Table 5.4 summarizes the synthesis results of the optical network interface using Reed-Solomon code RS(15,11,5). The total interface area of the transmitter and the receiver are $889\mu m^2$ and $3513.9\mu m^2$, respectively. The total power consumption is $19.2mW$, which is larger than the $9.5mW$ of the interface using Hamming codes due to the use of a more complex FEC.

The difference in E_b/N_0 (or SNR) to achieve a given BER of a given codec compared to the uncoded configuration is called coding gain. Figure 5.13 plots the BER performance as a function of the signal-to-noise ratio for the three codecs: RS(15,11,5), H(7,4) and

TABLE 5.4: Synthesis results of the proposed ONI using Reed-Solomon codes

TX	Amount	Critical Path (ns)	Total Area (μm^2)	Static Power (μW)	Dynamic Power (mW)	Total Power (mW)
RS Enc	1	0.4	251.3	3.28	1.190	1.200
DEMUX	1	0.03	762	10.69	1.45	1.46
Serializer	1	0.08	546.6	10	0.403	0.413
TX Allocator	1	0.09	90.10	0.843	0.072	0.073
RX	**Amount**	**Critical Path (ns)**	**Total Area (μm^2)**	**Static Power (μW)**	**Dynamic Power (mW)**	**Total Power (mW)**
RS Dec	1	0.4	2888.1	40.3	11.8	11.9
MUX	1	0.8	676	10.8	1.55	1.56
Deserializer	1	0.05	530.5	7.52	5.409	5.417
RX Allocator	1	0.09	95.3	1.07	0.171	0.172

H(71,64). As it can be noticed, at $BER = 10^{-12}$, the corresponding SNR of the channel with RS(15,11,5), H(7,4), and uncoded are 12.11 dB, 14.26 dB, and 16.94 dB, respectively. The result shows that the RS(15,11,5) provides the best coding gain (4.83 dB) compared to the other codecs due to its higher ability to correct the errors. Reed-Solomon code RS(15,11,5) can correct two errors whereas the Hamming code H(7,4) can correct only one error.

Typically, there is a trade-off between coding gain and decoder complexity. Some codes can provide higher BER performance, but also require higher power consumption, and similarly for decoding algorithms. RS(15,11,5) provides the best coding gain but the highest cost and power, whereas H(7,4) offers the lowest cost and power, but the lowest coding gain.

Communication Latency Along with the development of technology, latency is one of the essential factors of the growing interest in photonics interconnects. Indeed, the potentials of the optical network on chip rely on the properties of optical interconnects with high bandwidth, low latency, and less crosstalk noise. To exhaust all of the features of optical interconnects, the design of the ONI not only ensures energy efficiency but also adapts bandwidth and latency requirements. In detail, the interface is located between two frequency domains, and all the components must operate as fast as possible in order to adapt the modulation speed to the optical domain.

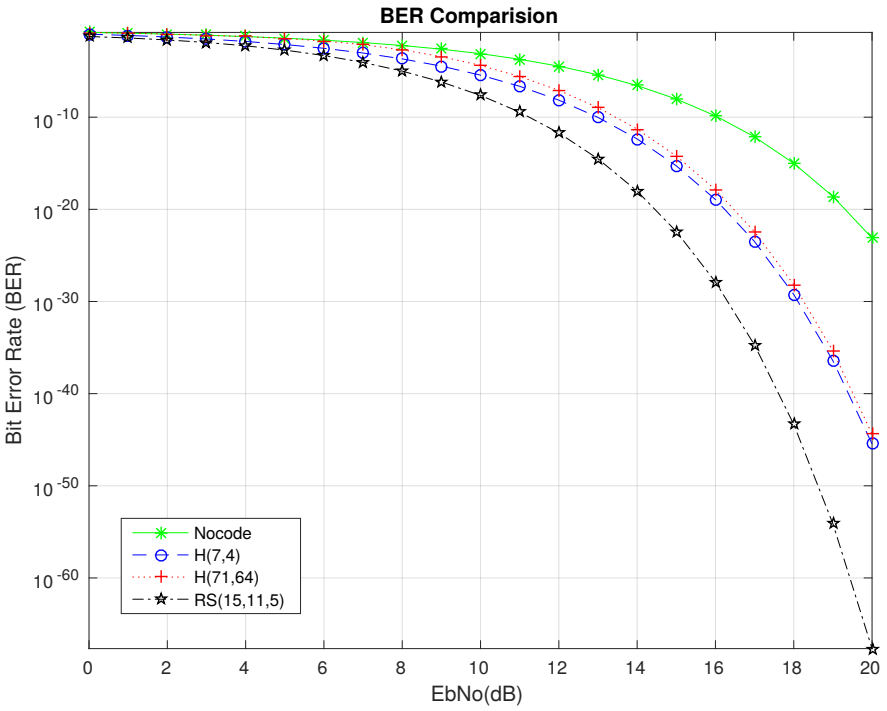


FIGURE 5.13: BER performance comparison between Hamming and Reed-Solomon codes

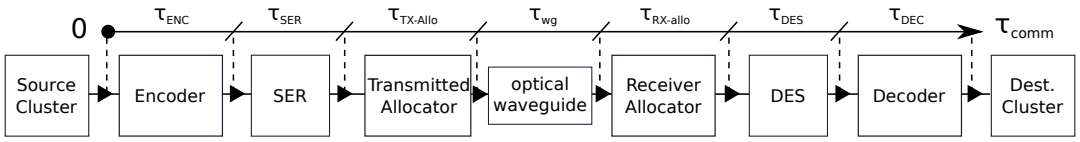


FIGURE 5.14: Communication latency of the proposed ONI using FECs

Figure 5.14 shows the different blocks and delays involved in a point-to-point on-chip optical link in our proposed architecture. Due to the potential complexity and cost of an implementation using FIFOs, we do not use FIFOs between the blocks. Instead, the transmitter must wait for several clock cycles until completion of previous data packet transfers. The time in which one packet is completely transferred from sender cluster to receiver cluster is called communication latency (τ_{comm}). Figure 5.14 also illustrate the communication latency of the optical interconnects based on the optical network interface designed in this chapter. As we can see in this figure, the communication latency accumulates the latency of FECs, SER/DES, and Transmitter/Receiver Allocator. Furthermore, the transfer delay of the optical signals into the waveguide must be considered[1]. The communication latency of the optical interface with the corresponded delay

[1]Delay in the optical waveguide depends on the communication distance and the material of the waveguide (from 0.023 ns to 0.320 ns [76])

of components is defined as

$$\tau_{comm} = \tau_{Enc/Dec} + \tau_{Ser/Des} + \tau_{TX-allo/RX-allo} + \tau_{wg}. \tag{5.1}$$

The latency values of the different elements are obtained from the synthesis results under 28 nm technology (Section 5.5.2). In this architecture, the most important factors contributing to the communication latency of the optical interconnects are the latency of SER and DES ($\tau_{Ser/Des}$) which are a function of number allocated wavelengths (N_{WL}). Indeed, the special structure of the proposed SER/DES allows for the WDM scheme to be used, and thus to allocate several wavelengths in a single waveguide to increase the bandwidth and reduce the communication latency. The allocation protocol can manage this configuration according to the application requirements. For instance, instead of using one wavelength for the connection, the management unit can configure eight wavelengths to increase the bandwidth and reduce the communication latency by eight.

We are studying the implementation in the interface of Hamming Codes and Reed-Solomon ECC. According to the implementation and synthesis results under 28 nm technology, a more accurate expression of the communication latency of the interface using Hamming codes as a function of the number allocated wavelengths is

$$\tau_{comm,H} = 2clk_e + \left(3 + \frac{nN}{kN_{WL}}\right) clk_o + \tau_{wg} \qquad \text{(ns)}, \tag{5.2}$$

where clk_e = 1 (ns) is the clock period in the electronic domain, clk_o = 0.1 (ns) is the clock period in the optical domain and N_{WL} is the number of allocated wavelengths. N is the number of data bits input. n and k are the code-word width and data input width of a single Hamming code H(n,k), respectively.

The latency of the interface using RS codes is expressed by

$$\tau_{comm,RS} = \left(80 + \frac{m(2^m - 1)}{N_{WL}}\right) clk_o + \tau_{wg} \qquad \text{(ns)}, \tag{5.3}$$

with m is the primitive polynomial of Galois field in Reed-Solomon codes.

Figure 5.15 plots the evaluation of the communication latency of the interface using Hamming H(7,4), H(71,64) and RS(15,11,5), respectively, as a function of the number of

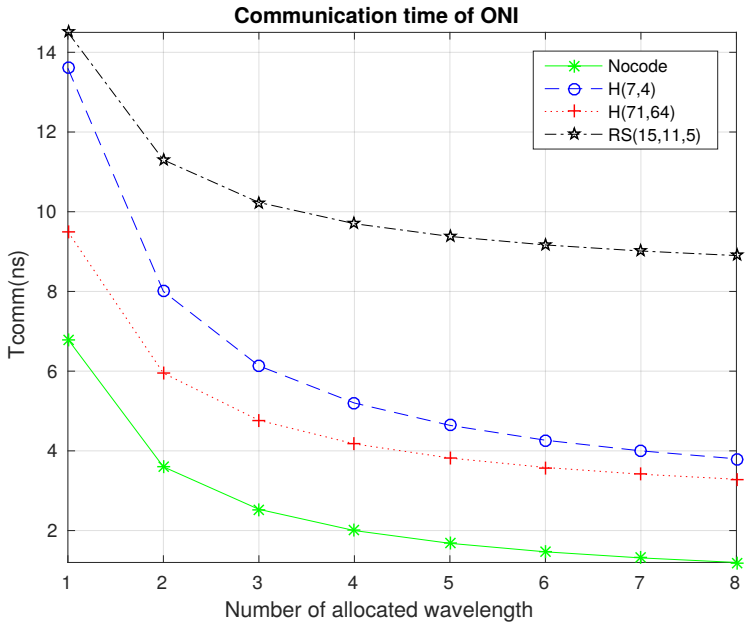


FIGURE 5.15: Communication latency (τ_{comm}) of the proposed ONI using various FECs or no FEC as a function of the number of allocated wavelengths

allocated wavelengths to send a message composed of 64 bits. According to the chart, the latency due to the interface using RS codes is the highest. This problem can be explained by the complexity of the decoder algorithm which can correct multiple errors compared to only one error with Hamming codes. In our implementation, the latency of RS(15,11,5) decoder takes 76 clock cycles with Berlekamp's algorithm decoding, whereas only one clock cycle is needed in the RS encoder. H(7,4) and H(71,64) show lower latency due to the simplification of the decoding algorithm. Interestingly, by using more wavelengths, the communication time can be significantly reduced.

On the other hand, due to the probability of correcting errors, Reed-Solomon codes can provide the best coding gain compared to the Hamming codes and thus give the best performance regarding energy efficiency. Therefore there exists a trade-off between the energy performance and the communication time which is addressed by the allocation part. This part is defined according to the application requirements. In this section, we focus on the actual architecture of the network interface and its evaluation. The trade-off between the unit control and the wavelengths allocation protocol has already been addressed in [63].

5.5.3 Laser Driver

Nowadays, optical network-on-chip are becoming a reality due to the feasible of the integration of optical devices with CMOS technology. The use of on-chip optical interconnects leads to higher bandwidth, lower latency and lower power consumption. In order to reduce the laser power and improve the performance of optical interconnects, we proposed the use of error correcting codes. In this method, the output power of the on-chip laser must be tuned according to match the expected propagation losses along the optical path. In this section, we will focus on the design of a laser driver for on-chip laser modulated by the direct method at a single wavelength of the optical signal.

There are many integrated laser devices like the Microdisk, VCSEL, and Distributed Brag Reflector. In this thesis, we will only focus on the VCSEL device due to its advantages. Compared to other integrated lasers, VCSEL has the capability of delivering the needed output power with the minimal integration area. VCSEL presents the good trade-off between area and power.

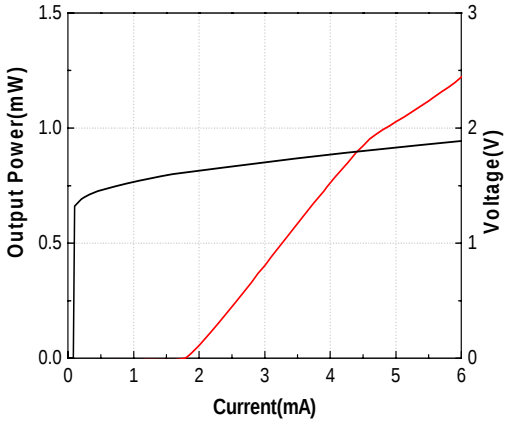


FIGURE 5.16: LIV curve of a VCSEL [17]

Figure 5.16 shows the behavior of a typical VCSEL [17]. In the direct modulation technique, the driver interfaces directly with the laser, hence the current intensity has to be changed to modulate the laser power. Different values of current are set up to create different levels of output powers that would represent a logical 1. Meanwhile, just only one bias current value was selected to represent a logical 0. This bias current is set as high as possible while getting an output power close to zero, to ensure fast dynamic switching between logical values. These values were the fundamental parameters for the design of the laser driver circuit.

In the context of optical modulation, On-Off Keying (OOK) coding is the simplest modulation technique which can adapt the communication speed and bandwidth requirements due to the simple implementation. In this method, logic '1' is represented by the presence of light in a given wavelength and logic '0' is an absence of light in this wavelength. This coding can be done by turn ON or turn OFF the laser directly.

5.5.3.1 Design of Laser Driver Circuit

In this section, we first introduce the methodology based on 28 nm FDSOI technology and then present the design of the multi-level driver. Finally, we discuss the results and the needed design procedure and some essential elements which impact the output current of laser power in this design.

5.5.3.2 Methodology and Tools

This section explores the methodology of the design under 28 nm FDSOI transistor technology which is provided by STMicroelectronics. This technology provides and supports a full design kit library that is compatible with Cadence software and is verified and tested on silicon. To perform circuit schematics and layout, we use Virtuoso schematic and layout tool. Also, Cadence provides a SPICE simulator (Spectre) to validate the performance of the integrated circuit design, by considering the transistor's dedicated technology parameters and model, which are well defined in the design kit library. By using Cadence, we can compute all the needed results regarding power and energy consumption. Moreover, we can extract node current and branch voltage values that are selected on the schematic design interface. This will also provide the designers with the needed tools like the eye diagram measurement tool to validate the signal quality and integrity. To verify our design performance, we can also extract the parasitic elements of our layout by using the Calibre tool that is also provided by Cadence and perform the post-layout simulation to confirm that the performance of the circuit is not degraded by the introduction of the circuit parasitic elements. With the use of the full set of tools provided by Cadence, the analog design procedure will be compact and time efficient.

Besides, To verify the driver circuit, we need a model of laser model which includes the load impedance characteristics. The load impedance is an important factor for the driver

design procedure, and we can extract different results from the same driver when interfaced with different load impedance characteristics. To simulate the device impedance, we use VerilogA model to describe the laser device as an impedance behaviour, by defining a polynomial function that relates the current and the voltage between two pins of laser that was extracted from the laser (V, I) curve. VerilogA [25] provides an extension for the Spice simulator, which can describe the analog and mixed-signal systems. As a result, we will get an analog behavioural model that is included in Spice simulation environment with other defined devices and components.

Similarly, in order to extract the results of the data modulation, we need a signal generator to provide the control signal for the driver input of transistors. According to the references, we use the LFSR (linear-feedback shift register) data generator in [85], this shift register can create a pseudo-random number generator to provide for the driver design. After synthesizing the code, we can extract the netlist and import the VHDL component back to the SPICE then use it likes the other defined components and devices.

5.5.3.3 Multi-Level Driver

By considering the advantages and disadvantages of some perspective designs, we illustrate the proposed design in Figure 5.17. The design can adapt to the communication data rate at 10 Gbps and provide good performance regarding area and power consumption. Figure 5.17 shows the schematic and principle of the proposed design which based on the multi-level concept. To obtain a two-level current output, the main tail current source of different pair consists of two transistors.

When both of the tail transistors are activated, we can achieve the worst case scenario current demands. However, if N5 is deactivated the logical high output current will decrease according to the current step which is directly related to the number of needed current levels. As for the footprint area budget, for each added output current level, we have to provide a separate transistor bias circuit and a deactivation CMOS transistor to pull low the voltage level at the gate of the desired tail transistor once we want to deactivate the current contribution of the biased current source.

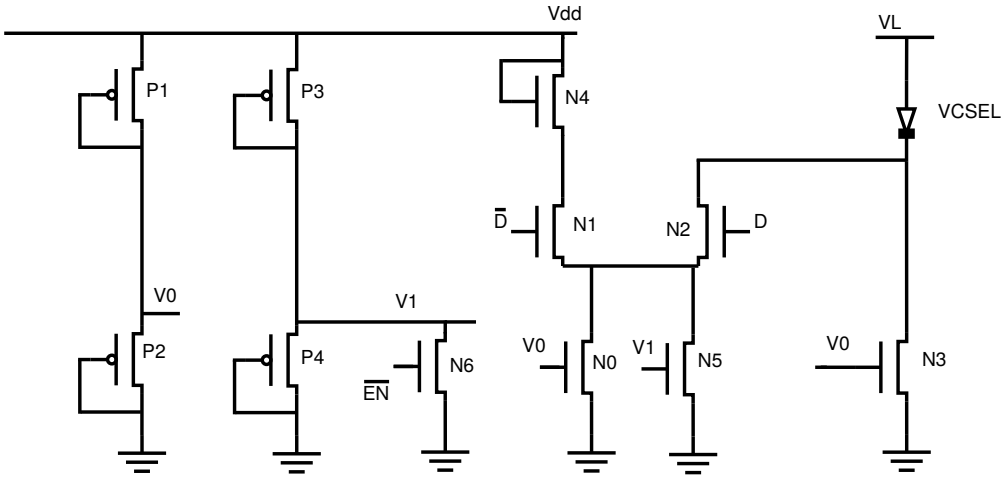


FIGURE 5.17: Multi-level driver design

Finally, we can confirm that this implementation of the multiple current level concept is scalable without having a significant impact on the footprint area and energy consumption budget. Having many output current levels can have a very beneficial effect on the whole optical link and network concerning efficiency and thermal manager. Thus proving that a dynamic driver approach is achievable without occupying an extensive footprint area to implement the needed hardware while maintaining the control circuitry as simple as possible to improve our overall system performance. We discuss in the next section the achieved results, the required design procedure and the most critical parameters that can affect our output current level.

5.5.3.4 Results

The design is simulated for three different scenarios corresponding to two, three, and five output current levels, respectively. Results are reported in Tables 5.5, 5.6, and 5.7. The current level can be changed according to the variation of current step C_{step} which is defined as

$$C_{step} = \frac{I_{max} - I_{min}}{N_{Levels}}. \tag{5.4}$$

TABLE 5.5: Energy efficiency with two-level output currents

Current Level (mA)	Driver Energy Consumption (pJ/bit)	Laser Energy Consumption (pJ/bit)
4.2	0.102	0.904
6	0.23	1.2

TABLE 5.6: Energy efficiency with three-level output currents

Current Level (mA)	Driver Energy Consumption (pJ/bit)	Laser Energy Consumption (pJ/bit)
3.6	0.0687	0.837
4.8	0.133	1.01
6	0.23	1.2

TABLE 5.7: Energy efficiency with five-level output currents

Current Level (mA)	Driver Energy Consumption (pJ/bit)	Laser Energy Consumption (pJ/bit)
3.12	0.045	0.77
3.84	0.08	0.87
4.5	0.115	0.96
5.21	0.16	1.06
6	0.23	1.2

Tables 5.5, 5.6, and 5.7 show that a considerable reduction in the energy consumption of the driver is achieved when the output current level is decreased. Therefore, by implementing the multi-level concept, we can save some energy consumption since the cost of additional hardware has a very minimal effect on the energy budget.

Figure 5.18 shows the relationship between the energy consumption and the output current from the synthesis results obtained for different levels of output current. It is obvious that energy consumption increases almost linearly according to the number of output levels. The chart demonstrates that the multi-level concept is scalable. Regarding the added hardware, Figure 5.19 illustrates the linear relationship between the number of output levels and the number of transistors used in this design.

Adjusting the bias voltage for the different current can reduce the number of adjustable parameters and the output level variation. However, it will also reduce the complexity of the whole design since we do not have to provide the needed voltage source for each of them. Moreover, in our proposed technique, we simplified and ensured that all the required voltage sources could be supplied from the primary power source that falls into the technology limit. Hence, we rely on the physical dimensions of the transistors, which limits our post fabrication intervention.

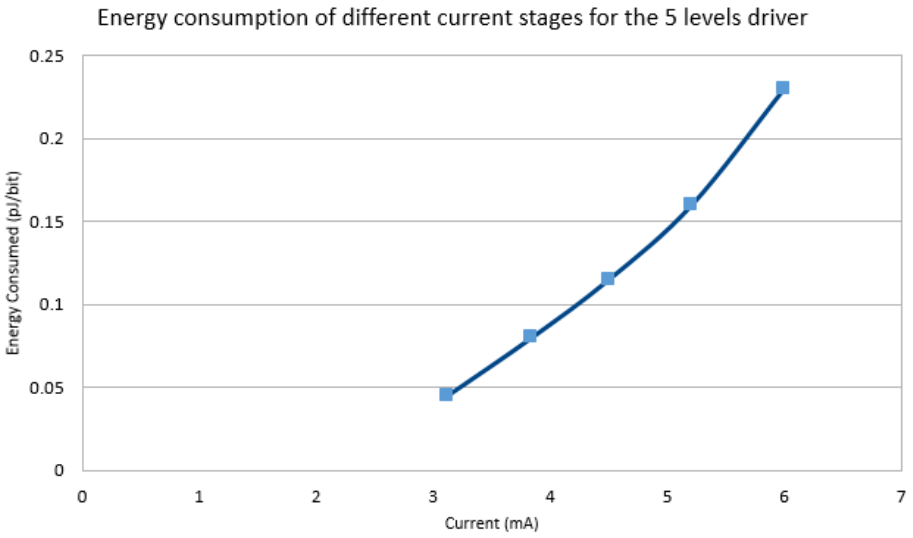


FIGURE 5.18: Relation between the energy consumption and the current level

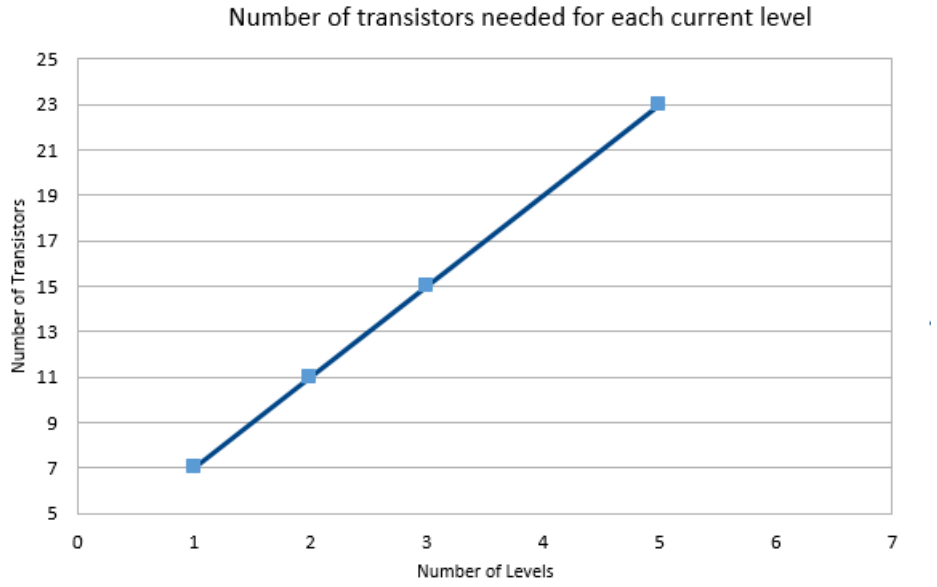


FIGURE 5.19: Relation between the number of current levels and number of used transistors

5.5.4 ONI Manager

The Optical Network Interface Manager (OM) located at each ONI configures the transmitter and the receiver. It includes an ONI configuration memory which stores all the configurations to control the MR and Laser power at different operating modes and different steps composing a sequence of configurations.

In this section, we present the design and hardware implementation of the ONI manager

under 28 nm technology. Figure 5.20 shows the overview of the design and its configuration memory. The input "$Mode$" is taken from the output "$Change-config$" of OCS block (see section 5.5.5). In this design, we assume that there are only three modes automatically generated by the framework in [61]: High Performance, Balance and Low Power. These modes are illustrated in Figure 5.20.b by three rectangles in blue, green, and red, respectively. The input "$Current-step$" is taken from the internal counter of OCS. With this input, the ONI manager can know when the communications are finished and prepare setting up for communication of the next steps. The outputs of the ONI manager are connected to MR and Laser source in three ways. The first one (MR_{RX}) is connected to the MRs in the receiver to drop out the optical signal from the waveguide. The second one (MR_{TX}) is used for configuration the MRs in the transmitter to inject the signal from the laser source into the waveguide. The last one (P_{Laser}) is the control input of the laser power driver. This input indicates which level of laser power is emitted to adapt the communication requirements.

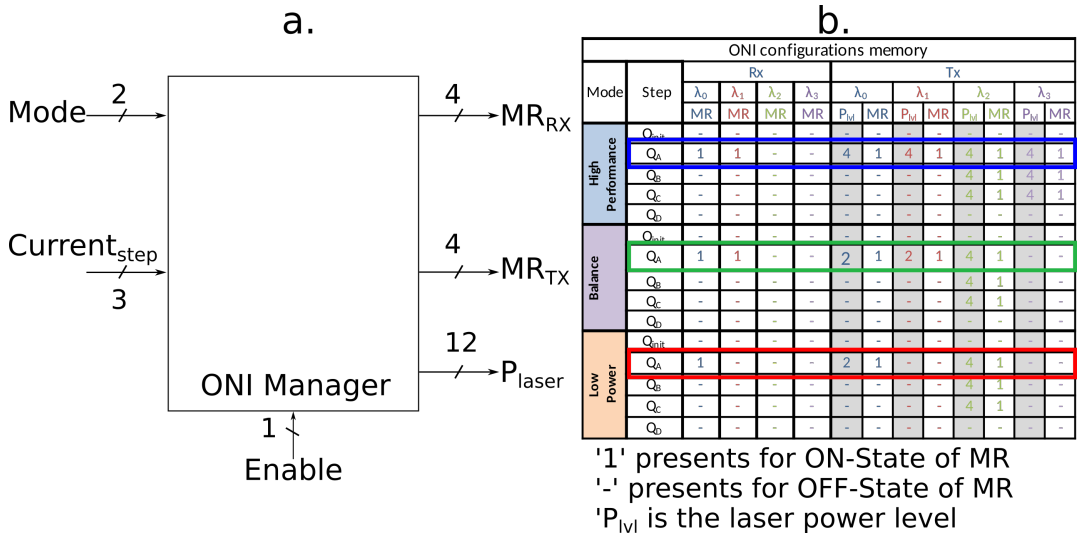


FIGURE 5.20: ONI manager and its configuration memory

Figure 5.21 shows the simulation result of an ONI manager, in which, we assume four ONIs, four wavelengths, and five configurable levels of electrical laser power: 3.12mW, 3.84mW, 4.5mW, 5.21mW, and 6mW (see Table 5.7). As we can see in the blue rectangle of Figure 5.21, the values of MR_{TX}, MR_{RX} and P_{Laser} are 15, 12 and 2340, which corresponds to the configuration of step QA at HP mode. Similar results are obtained with the other cases of configuration mode. Finally, the configuration can be applied to the ONIs as illustrated in the bottom of Figure 5.21. First, optical channels are opened by switching ON the involved MRs in the transmitter and the receiver. Second, the power of

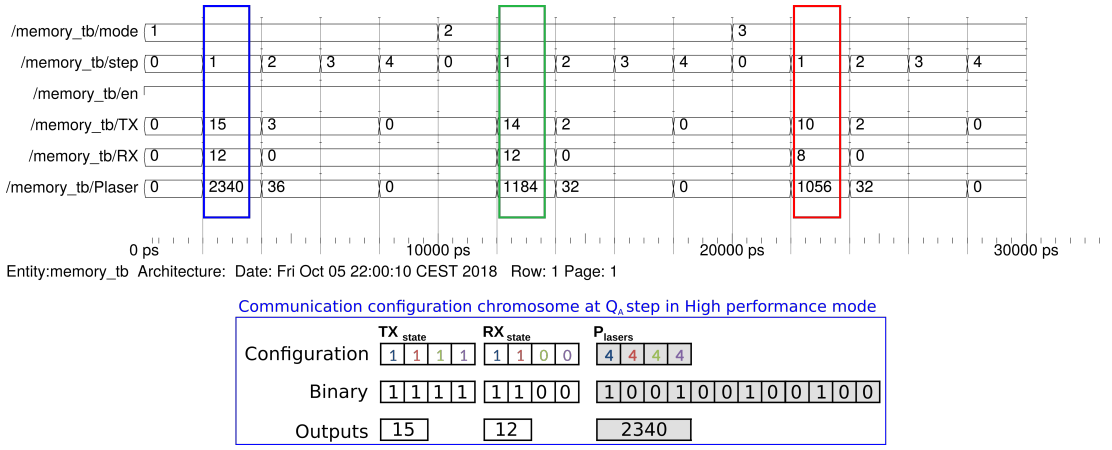


FIGURE 5.21: Manager ONI simulation result

the optical signals propagating through the channels is defined according to the selected lasers power level. It is clear to see that the result demonstrates the correct principle of the proposed ONI Manager.

TABLE 5.8: Synthesis results of ONI manager according to number of MRs and the level of laser power

Number of Modes	Level of Laser Power	Number of MRs	Synthesis Reports				
			Total Area (μm)	Static Power (μW)	Internal Power (μW)	Switching Power (nW)	Total Power (μW)
3	5	4	30.028	0.6055	0.0163	5.018	0.6268
		8	42.59	0.9688	0.02561	7.252	1.002
		16	63.158	1.313	0.03393	10.05	1.357
		32	85.843	1.873	0.05215	9.817	1.935
		64	172.50	3.463	0.1212	19.22	3.604

Furthermore, Table 5.8 shows the synthesis results of the ONI manager with a different number of MRs. We can conclude from these results that the proposed design is scalable with negligible effect on the footprint area and energy consumption. The results demonstrate that the design is deployable in a wide range of sizes and configurations. Finally, the OCS supports the run-time management of energy-performance trade-off.

5.5.5 ONoC Configuration Sequencer

In this section, we present the architecture of the ONoC configuration sequencer (OCS) in charge of synchronizing all the ONI Managers of the ONoC. Figure 5.22 shows the general architecture of OCS which includes a counter, an enable block, a mode configuration memory and a comparator. The input signal of OCS comes from the Operating System to

select the configuration mode satisfying application requirements. Moreover, the outputs of OCS are connected to the ONIs through two signals: The first is a signal generated by the counter indicating that a step is over. The bit-width of this signal depends on the maximum number of steps in all modes. The second signal bit-width depends on the number of modes embedded in the ONI configuration memory located at each ONIs.

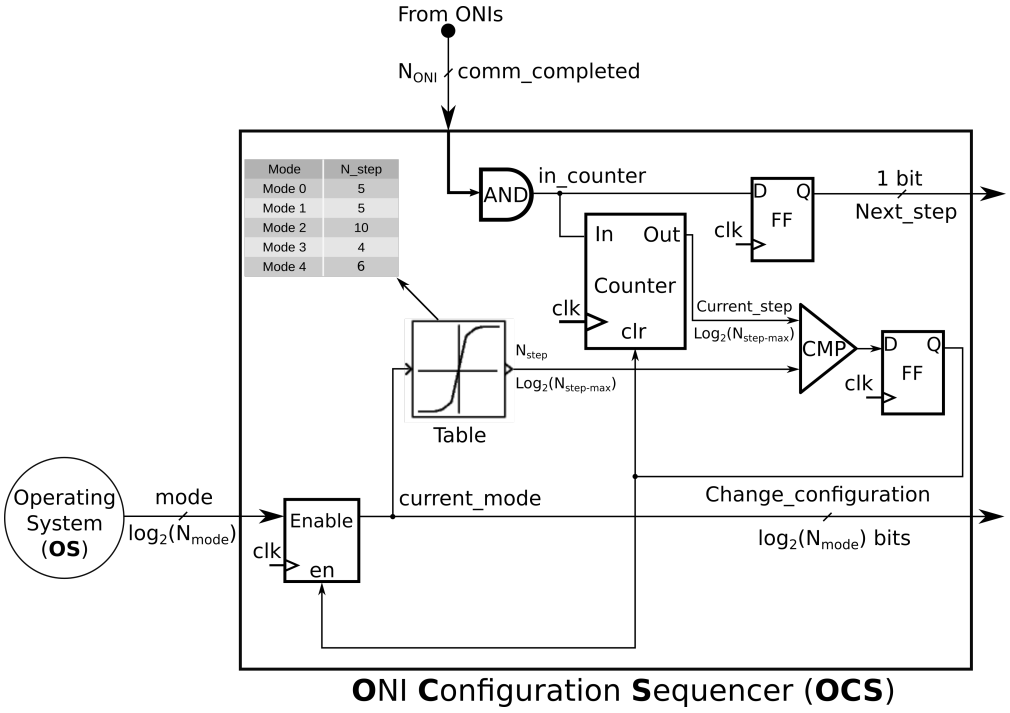


FIGURE 5.22: The general architecture of the optical network interface configuration sequencer

In Figure 5.22, we assume that the modes are generated by the framework from [61]. With this framework, we can extract the configuration modes with any parameter from ONoC. For instance, Table 5.9 reports five modes with different configurations in term of energy and performance. Among them, Mode 2 has the maximum number of steps with 10 steps.

TABLE 5.9: Example of ONoC configuration modes

Modes	Number of Steps
Mode 0	5
Mode 1	5
Mode 2	10
Mode 3	4
Mode 4	6

The number of modes is a parameter that indicates the number bits of the counter (in this case, we need 4 bits width to count up to 10 steps). Therefore, the number of modes

contributes to the hardware cost as well as the power consumption and the area of the design. The OCS counter receives the agreement signal (all of the communications are completed) from all ONIs to activate the counter begin to count until the maximum step. Then, the output of the comparator is set at the high level to reset the counter and enable to set up the configuration for ONIs. Finally, the current mode is connected to all the corresponded ONIs to configure the transmitters and receivers.

Figure 5.23 shows the simulation result of the OCS connected with eight ONIs and the number of configuration presented in table 5.9 with the corresponded number of steps. The simulation demonstrates the correct principle of the proposed OCS. In the next section, we present the synthesis results of OCS in different parameters of ONoC.

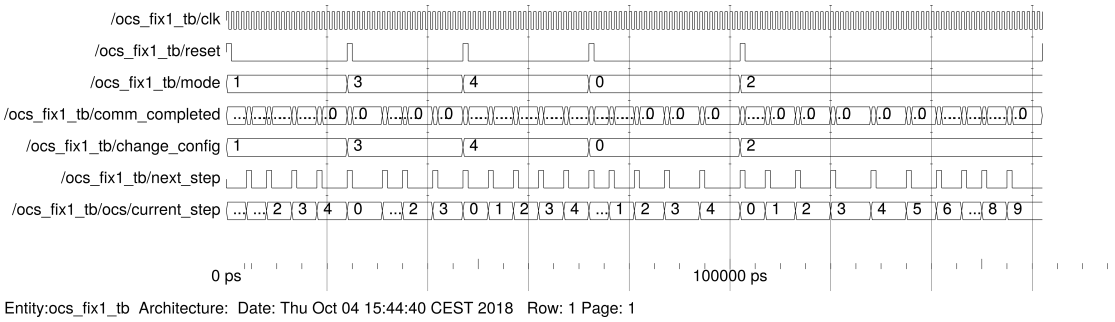


FIGURE 5.23: Simulation of the OCS

5.5.5.1 Results

With the proposed design, the communication requirements and operation of the interface are adapted. In this section, we present the synthesis results of OCS for various resource and input parameters. The results are synthesized under 28 nm FDSOI technology. Table 5.10 shows the comparison of OCS synthesis results according to the number of ONIs, the number of modes as well as the number of steps at each mode. The power consumption is not significantly impacted with 21.13 μW, 21.27 μW and 21.56 μW when the number of ONIs equal to 8, 16 and 32, respectively. However, there is a slight increase in power consumption (2,4 %) when the number of steps at a given mode increases from 10 up to 1024 steps. Especially, when the number of modes increases from 5 to 32 modes, a 31.25 % increase in total power is shown, although staying not significant in the overall ONI power budget.

TABLE 5.10: Synthesis results of the OCS according to number of ONIs and number of modes

Number of ONIs	Number of Modes	Number of Steps	Synthesis Reports				
			Critical Path (ns)	Total Area (μm)	Static Power (μW)	Dynamic Power (μW)	Total Power (μW)
8	5	10	0.89	41.126	0.8276	20.3	21.13
	5	128	0.80	67.075	1.241	33.00	34.25
	5	1024	0.73	92.371	1.604	51.40	53.02
	16	10	0.89	35.577	0.7269	20.6	21.37
	16	512	0.76	70.176	1.212	43.8	44.99
	16	1024	0.73	77.030	1.331	51.3	52.62
	32	10	0.89	35.904	0.7635	42.0	42.74
16	5	10	0.89	44.553	0.8296	20.3	21.17
	5	128	0.80	70.502	1.253	33.2	34.45
	5	1024	0.73	95.798	1.615	53.0	54.59
	16	10	0.89	39.004	0.7392	20.7	21.48
	16	512	0.76	73.603	1.224	44.5	45.75
	16	1024	0.73	80.457	1.342	52.7	54.04
	32	10	0.89	39.331	0.7757	42.2	42.97
32	5	10	0.89	51.408	1.142	20.4	21.56
	5	128	0.80	77.356	1.548	33.6	35.14
	5	1024	0.73	102.65	0.7392	20.7	21.48
	16	10	0.89	45.859	1.044	21.0	22.00
	16	512	0.76	80.457	1.452	46.1	47.59
	16	1024	0.73	73.929	1.266	50.3	51.56
	32	10	0.89	46.185	1.068	42.6	43.71

It is clear that the area increases with the number ONIs from 8 to 16 and 32. Furthermore, the total area is almost twice when the number of steps increases from 10 to 1024 steps. Similarly, the number of modes does not significantly impact the area thanks to the simple architecture of the OCS. Finally, the critical path obtained demonstrates that all of the OCS can operate at 1 Ghz frequency in the electrical domain. As a conclusion, we can confirm that this implementation of the proposed design is scalable without having a great impact on the footprint area and energy consumption budget of the overall ONI. The results demonstrate that the design is deployable in a wide range of sizes and configurations.

5.6 Conclusion

In this chapter we presented a method to offer dynamicity to ONoC in terms of energy versus performance trade-offs. The hardware blocks in charge of the run-time management of the ONoC have been presented and the method generates the allocation solution through an offline optimizing framework. The ONoC dynamicity is exploited by the Operating System regarding the application requirements. An off line analyze of the application mapped on the architecture allows to extract all the possible configurations to support the communications Based on this analyze, a sequence of communication configurations is then controlled step by step by the Operating System to ensure the current requirements.

This dynamicity in the ONoC is closely linked to the use of the proposed ONI. We shown that our ONI is composed of several parts enhancing the efficiency of the ONoCs. The proposed ONI is scalable and meets all the constraint need by the association of electrical and opctical domains.

Chapter 6

Conclusions and Perspectives

3D Optical Network-on-Chip is probably one interesting emerging technology for the future generation of on-chip interconnects. Indeed, this technology provides several advantages such as low latency, high bandwidth and high energy efficiency properties. Furthermore, wavelength multiplexing division (WDM) technique can be used to allocate several wavelengths for one specific communication leading to improve the bandwidth and to reduce the latency for data exchanges between IP cores. This technique can lead to the appearance of attenuation and crosstalk noise for optical signals, and in this case, it can reduce energy efficiency and increase the Bit Error Rate of the overall system. To address these issues, we present in this thesis some energy efficiency improvements through the following aspects.

Firstly, we model and analyze the optical losses and crosstalk for WDM used in ONoC. The model provides an analytic evaluation of the worst case of loss and crosstalk with different parameters for the optical ring topology. More precisely, based on the Chameleon architecture, both worst-case loss and average loss are modelled for a different number of IP cores. Results prove that the loss and crosstalk noise in Chameleon less impact the energy compared to the state-of-the-art in ONoC. This feature can be obtained thanks to the ring topology, the regular layout of the optical interface and the multi-layer technology.

Secondly, based on this model of attenuation and crosstalk, we propose a methodology to improve the performance and then to reduce the power consumption of optical interconnects relying on the use of forward error correction (FEC). We present two case studies of

lightweight FEC with low implementation complexity and high error-correction performance. We also present the hardware blocks supporting FEC which have been developed under 28nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology. More precisely, based on Chameleon architecture defined for 4x4 IPs size, and for the following parameters: number of wavelengths equal to $N_{wavelength}$ = 4, laser efficiency $Laser_{eff}$ = 5%, worse case of losses L_{wc} = 3.25(dB), BER = 10^{-12}, and for Hamming codes (7,4) and Reed-Solomon RS(15,11,5) FEC, our solution leads to energy saving equal to 71.1 % and 80.3 % respectively. Regarding this power saving, RS shows its ability to become the best candidate compared to Hamming codes. Furthermore, we also present the trade-off between the BER and laser power at the range of BER from 10^{-4} to 10^{-12}. The results demonstrate the potential of the proposed approach to overcome performance and power issues of the optical interconnect in the context of the ONoC.

Thirdly, a complete design of Optical Network Interface (ONI) is presented to support, at run-time, all communication schemes of Chameleon architecture. This optical interface is composed of FECs hardware blocks: data serialization/deserialization, allocator and laser power management. The hardware implementation and synthesis results show the scalability of the interface and demonstrate that the design is deployable in a wide range of sizes and configurations. Relying on this network interface, an allocation management block to improve energy efficiency can be supported at runtime in order to adapt the application requirements. This run-time management of energy vs performance can be integrated into the ONI manager through configuration manager located in each ONI. Moreover, the design of an ONoC configuration sequencer (OCS), located at the center of the optical layer, is presented. By using the ONI manager, the OCS can configure the ONoC at run-time according to the application performance and energy requirements.

However, several future works based on the proposed techniques and contributions in this thesis can be foreseen.

In order to improve the energy efficiency of ONoC, a run-time configuration of laser power based on the communication requirements will be further developed by considering the energy consumption of each communication. A global ECC configuration algorithm could also be developed to manage the parameters of all the communications of the system. To evaluate this perspective, we will further investigate the achievable energy efficiency

improvement by simulating the execution of standard benchmark applications on nano-photonic interconnects.

As discussed in state of the art, thermal dissipation is one of the most important issues contributing to the overall system performance. Indeed, thermal effects can lead to MR resonance wavelength drift, which is the main reason for errors and loss along the communication path. In order to reduce the impact of this problem, we will investigate an algorithm to manage the laser power by taking the thermal issue into account. In particular, this algorithm can be integrated into a more intelligent ONI manager considering the trade-off between the thermal problem and the energy efficiency. Then, hardware implementation and synthesis of the algorithm will thus be studied. To do this, an analytic model of attenuation and crosstalk when considering the thermal effect must be carefully addressed. Furthermore, to improve the sensitivity of the receiver to adapt the requirement of the multi-current transmitter, the design of multilevel receiver needs to be considered too.

Finally, the global architecture composed of a set of clusters connected by ONoC needs to be considered and studied. More precisely, the size of the clusters, the organization of the network, the number of waveguides and wavelengths, the number of level for laser powers, etc, have to be determined, with respects to the energy, performance, and thermal constraints. These different parameters are not all independent, and a trade-off between them needs to be studied in order to optimize the general performances of the system.

Author's Publications

The following publications have been co-authored by the author of this thesis and partly rely on this thesis work [64], [43], [60], [63], [82], [83].

Bibliography

[1] A. K. Dutta *et al. WDM technologies: optical networks.* Academic Press, 2004.

[2] M. Bahadori, R. Polster, S. Rumley, Y. Thonnart, J. L. Gonzalez-Jimenez, and K. Bergman. Energy-bandwidth design exploration of silicon photonic interconnects in 65nm cmos. In *2016 IEEE Optical Interconnects Conference (OI)*, pages 2–3, May 2016.

[3] M. Bahadori, S. Rumley, D. Nikolova, and K. Bergman. Comprehensive design space exploration of silicon photonic interconnects. *Journal of Lightwave Technology*, 34(12), June 2016.

[4] C. Batten, A. Joshi, V. Stojanovic, and K. Asanovic. Designing chip-level nanophotonic interconnection networks. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2(2):137–153, June 2012.

[5] Guido Belfiore, Laszlo Szilagyi, Ronny Henker, and Frank Ellinger. Low power laser driver design in 28nm cmos for on-chip and chip-to-chip optical interconnect. In *Proc. SPIE*, pages 9662 – 9662 – 8, 2015.

[6] J.M. Berger. A note on error detection codes for asymmetric channels. *Information and Control*, 4(1):68 – 73, 1961.

[7] Keren Bergman, Luca P. Carloni, Aleksandr Biberman, Johnnie Chan, and Gilbert Hendry. *Photonic Network-on-Chip Design*, volume 68 of *Integrated Circuits and Systems*. Springer, 2014.

[8] C. Berrou, A. Glavieux, and P. Thitimajshima. Near shannon limit error-correcting coding and decoding: Turbo-codes. 1. In *Communications, 1993. ICC '93 Geneva. Technical Program, Conference Record, IEEE International Conference on*, volume 2, pages 1064–1070 vol.2, May 1993.

[9] S. Le Beux, J. Trajkovic, I. O'Connor, and G. Nicolescu. Layout guidelines for 3d architectures including optical ring network-on-chip (ornoc). In *2011 IEEE/IFIP 19th International Conference on VLSI and System-on-Chip*, pages 242–247, Oct 2011.

[10] Aleksandr Biberman, Kyle Preston, Gilbert Hendry, Nicolás Sherwood-Droz, Johnnie Chan, Jacob S. Levy, Michal Lipson, and Keren Bergman. Photonic network-on-chip architectures using multilayer deposited silicon materials for high-performance chip multiprocessors. *J. Emerg. Technol. Comput. Syst.*, 7(2):7:1–7:25, July 2011.

[11] M. Briere, B. Girodias, Y. Bouchebaba, G. Nicolescu, F. Mieyeville, F. Gaffiot, and I. O'Connor. System level assessment of an optical noc in an mpsoc platform. In *2007 Design, Automation Test in Europe Conference Exhibition*, pages 1–6, April 2007.

[12] J. Van Campenhout, L. Liu, P. Rojo Romeo, D. Van Thourhout, C. Seassal, P. Regreny, L. D. Cioccio, J. M. Fedeli, and R. Baets. A compact soi-integrated multiwavelength laser source based on cascaded inp microdisks. *IEEE Photonics Technology Letters*, 20(16):1345–1347, Aug 2008.

[13] Long Chen, Po Dong, and Michal Lipson. High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding. *Opt. Express*, 16(15):11513–11518, Jul 2008.

[14] Long Chen and Michal Lipson. Ultra-low capacitance and high speed germanium photodetectors on silicon. *Opt. Express*, 17(10):7901–7906, May 2009.

[15] Xuemin Chen. *Error-Control Coding for Data Networks.* Kluwer Academic Publishers, Norwell, MA, USA, 1999.

[16] Alessandro Cilardo and Edoardo Fusella. Design automation for application-specific on-chip interconnects: A survey. *Integration, the VLSI Journal*, 52:102–121, 2016.

[17] Optowell Co. Ss85-5u001 850nm vcsel chip for sensor datasheet.

[18] P. Dong, W. Qian, S. Liao, H. Liang, C. C. Kung, N. N. Feng, R. Shafiiha, J. Fong, D. Feng, A. V. Krishnamoorthy, and M. Asghari. Low loss silicon waveguides for

application of optical interconnects. In *IEEE Photonics Society Summer Topicals 2010*, pages 191–192, July 2010.

[19] P. Dong, W. Qian, S. Liao, H. Liang, C. C. Kung, N. N. Feng, R. Shafiiha, J. Fong, D. Feng, A. V. Krishnamoorthy, and M. Asghari. Low loss silicon waveguides for application of optical interconnects. In *IEEE Photonics Society Summer Topicals 2010*, pages 191–192, July 2010.

[20] L.H.K. Duong, M. Nikdast, S. Le Beux, Jiang Xu, Xiaowen Wu, Zhehui Wang, and Peng Yang. A case study of signal-to-noise ratio in ring-based optical networks-on-chip. *Design Test, IEEE*, 31(5):55–65, Oct 2014.

[21] A. W. Fang, B. R. Koch, R. Jones, E. Lively, D. Liang, Y. H. Kuo, and J. E. Bowers. A distributed bragg reflector silicon evanescent laser. *IEEE Photonics Technology Letters*, 20(20):1667–1669, Oct 2008.

[22] Alexander W. Fang, Hyundai Park, Oded Cohen, Richard Jones, Mario J. Paniccia, and John E. Bowers. Electrically pumped hybrid algainas-silicon evanescent laser. *Opt. Express*, 14(20):9203–9210, Oct 2006.

[23] Nathan Farrington, George Porter, Sivasankar Radhakrishnan, Hamid Hajabdolali Bazzaz, Vikram Subramanya, Yeshaiahu Fainman, George Papen, and Amin Vahdat. Helios: A hybrid electrical/optical switch architecture for modular data centers. In *Proceedings of the ACM SIGCOMM 2010 Conference*, SIGCOMM '10, pages 339–350, New York, NY, USA, 2010. ACM.

[24] J. Faucher, M. B. Venditti, and D. V. Plant. Application of parallel forward-error correction in two-dimensional optical-data links. *Journal of Lightwave Technology*, 21(2):466–475, Feb 2003.

[25] Dan FitzPatrick and Ira Miller. *Analog Behavioral Modeling with the VERILOG-a Language*. Kluwer Academic Publishers, Norwell, MA, USA, 1st edition, 1997.

[26] C. Fougstedt, K. Szczerba, and P. Larsson-Edefors. Low-power low-latency bch decoders for energy-efficient optical interconnects. *Journal of Lightwave Technology*, 35(23):5201–5207, Dec 2017.

[27] E. Fusella and A. Cilardo. Lighting up on-chip communications with photonics: Design tradeoffs for optical noc architectures. *IEEE Circuits and Systems Magazine*, 16(3):4–14, thirdquarter 2016.

[28] M. Georgas, J. Leu, B. Moss, C. Sun, and V. Stojanovifá. Addressing link-level design tradeoffs for integrated photonic interconnects. In *2011 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–8, Sept 2011.

[29] Ryan Going, Tae Joon Seok, Jodi Loo, Kyle Hsu, and Ming C. Wu. Germanium wrap-around photodetectors on silicon photonics. *Opt. Express*, 23(9):11975–11984, May 2015.

[30] V. D. Gol and E. K. Tsmykal. Forward error correction in dwdm fiber-optic transmission system. *Radioelectronics and Communications Systems*, 52(6):317–323, Jun 2009.

[31] W. D. Grover. Forward error correction in dispersion-limited lightwave systems. *Journal of Lightwave Technology*, 6(5):643–654, May 1988.

[32] H. Gu and J. Xu. Design of 3d optical network on chip. In *2009 Symposium on Photonics and Optoelectronics*, pages 1–4, Aug 2009.

[33] Huaxi Gu, Jiang Xu, and Wei Zhang. A low-power fat tree-based optical network-on-chip for multiprocessor system-on-chip. In *2009 Design, Automation Test in Europe Conference Exhibition*, pages 3–8, April 2009.

[34] K. Guan, B. S. G. Pillai, A. Vishwanath, D. C. Kilper, and J. Llorca. The impact of error control on energy-efficient reliable data transfers over optical networks. In *2013 IEEE International Conference on Communications (ICC)*, pages 4083–4088, June 2013.

[35] R. Ho, K.W. Mai, and M.A. Horowitz. The future of wires. *Proceedings of the IEEE*, 89(4):490–504, Apr 2001.

[36] Sheryl L. Howard, Christian Schlegel, and Kris Iniewski. Error control coding in low-power wireless sensor networks: When is ecc energy-efficient? *EURASIP J. Wirel. Commun. Netw.*, 2006(2):29–29, April 2006.

[37] Zhihong Huang, Cheng Li, Di Liang, Kunzhi Yu, Charles Santori, Marco Fiorentino, Wayne Sorin, Samuel Palermo, and Raymond G. Beausoleil. 25gbps low-voltage waveguide si-ge avalanche photodiode. *Optica*, 3(8):793–798, Aug 2016.

[38] Tsutomu Ishi, Junichi Fujikata, Kikuo Makita, Toshio Baba, and Keishi Ohashi. Si nano-photodiode with a surface plasmon antenna. *Japanese Journal of Applied Physics*, 44(3L):L364, 2005.

[39] J. Jeddeloh and B. Keeth. Hybrid memory cube new dram architecture increases density and performance. In *2012 Symposium on VLSI Technology (VLSIT)*, pages 87–88, June 2012.

[40] A. Joshi, C. Batten, Y. J. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanovic. Silicon-photonic clos networks for global on-chip communication. In *2009 3rd ACM/IEEE International Symposium on Networks-on-Chip*, pages 124–133, May 2009.

[41] S. Kasnavi, S. Kilambi, B. Crowley, K. Iniewski, and B. Kaminska. Application of error control codes (ecc) in ultra-low power rf transceivers. In *2005 IEEE Dallas/CAS Workshop on Architecture, Circuits and Implementtation of SOCs*, pages 195–198, Oct 2005.

[42] M. Kennedy and A. K. Kodi. Laser pooling: Static and dynamic laser power allocation for on-chip optical interconnects. *Journal of Lightwave Technology*, 35(15):3159–3167, Aug 2017.

[43] Cedric Killian, Daniel Chillet, Sébastien Le Beux, Olivier Sentieys, Van Dung Pham, and Ian O'Connor. Energy and performance trade-off in nanophotonic interconnects using coding techniques. In *DAC 2017 - IEEE/ACM Design Automation Conference DAC*, page 6, Austin, United States, June 2017.

[44] N. Kirman, M. Kirman, R. K. Dokania, J. F. Martinez, A. B. Apsel, M. A. Watkins, and D. H. Albonesi. Leveraging optical technology in future bus-based chip multiprocessors. In *2006 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'06)*, pages 492–503, Dec 2006.

[45] I. Kiyat, A. Aydinli, and N. Dagli. Low-power thermooptical tuning of soi resonator switch. *IEEE Photonics Technology Letters*, 18(2):364–366, Jan 2006.

[46] TL Koch. Opportunities and challenges in silicon photonics. In *LEOS 2006-19th Annual Meeting of the IEEE Lasers and Electro-Optics Society*, 2006.

[47] P. Koka, M. O. McCracken, H. Schwetman, C. H. O. Chen, X. Zheng, R. Ho, K. Raj, and A. V. Krishnamoorthy. A micro-architectural analysis of switched photonic multi-chip interconnects. In *2012 39th Annual International Symposium on Computer Architecture (ISCA)*, pages 153–164, June 2012.

[48] George Kurian, Jason E. Miller, James Psota, Jonathan Eastep, Jifeng Liu, Jurgen Michel, Lionel C. Kimerling, and Anant Agarwal. Atac: A 1000-core cache-coherent processor with on-chip optical network. In *Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques*, PACT '10, pages 477–488, New York, NY, USA, 2010. ACM.

[49] L. H. K. Duong *et al.* Coherent and incoherent crosstalk noise analyses in inter-chip/intrachip optical interconnection networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pages 2475–2487, July 2016.

[50] S. Lardenois, D. Pascal, L. Vivien, E. Cassan, S. Laval, R. Orobtchouk, M. Heitzmann, N. Bouzaida, and L. Mollard. Low-loss submicrometer silicon-on-insulator rib waveguides and corner mirrors. *Opt. Lett.*, 28(13):1150–1152, Jul 2003.

[51] S. Le Beux, Hui Li, I. O'Connor, K. Cheshmi, Xuchen Liu, J. Trajkovic, and G. Nicolescu. Chameleon: Channel efficient optical network-on-chip. In *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014*, pages 1–6, March 2014.

[52] S. Le Beux, Hui Li, I. O'Connor, K. Cheshmi, Xuchen Liu, J. Trajkovic, and G. Nicolescu. Chameleon: Channel efficient optical network-on-chip. In *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014*, pages 1–6, March 2014.

[53] S. Le Beux, J. Trajkovic, I. O'Connor, G. Nicolescu, G. Bois, and P. Paulin. Optical ring network-on-chip (ornoc): Architecture and design methodology. In *Design, Automation Test in Europe Conference Exhibition (DATE), 2011*, pages 1–6, March 2011.

[54] Sébastien Le Beux, Jelena Trajkovic, Ian O'Connor, Gabriela Nicolescu, Guy Bois, and Pierre Paulin. System level exploration for the integration of optical networks

on chip in 3d mpsoc architectures. In Ian O'Connor and Gabriela Nicolescu, editors, *Integrated Optical Interconnect Architectures for Embedded Systems*, pages 241–261. Springer New York, New York, NY, 2013.

[55] C. Li, C. H. Chen, B. Wang, S. Palermo, M. Fiorentino, and R. G. Beausoleil. An energy-efficient silicon microring resonator-based photonic transmitter. *IEEE Design Test*, 31(5):46–54, Oct 2014.

[56] H. Li, A. Fourmigue, S. Le Beux, X. Letartre, I. O'Connor, and G. Nicolescu. Thermal aware design method for vcsel-based on-chip optical interconnect. In *2015 Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 1120–1125, March 2015.

[57] H. Li, A. Fourmigue, S. Le Beux, I. O'Connor, and G. Nicolescu. Towards maximum energy efficiency in nanophotonic interconnects with thermal-aware on-chip laser tuning. *IEEE Transactions on Emerging Topics in Computing*, PP(99):1–1, 2016.

[58] Shu Lin and Daniel J. Costello. *Error Control Coding, Second Edition.* Prentice-Hall, Inc., Upper Saddle River, NJ, USA, 2004.

[59] M. Lipson. Guiding, modulating, and emitting light on silicon-challenges and opportunities. *Journal of Lightwave Technology*, 23(12):4222–4238, Dec 2005.

[60] Jiating Luo, A Elantably, V. D. Pham, C Killian, Daniel Chillet, S Le Beux, Olivier Sentieys, and I O 'connor. Performance and Energy Aware Wavelength Allocation on Ring-Based WDM 3D Optical NoC. In *Design, Automation & Test in Europe Conference & Exhibition (DATE 2017)*, Lausanne, Switzerland, March 2017.

[61] Jiating Luo, Cedric Killian, Sebastien Le Beux, Daniel Chillet, Olivier Sentieys, and Ian O'Connor. Offline optimization of wavelength allocation and laser power in nanophotonic interconnects. *J. Emerg. Technol. Comput. Syst.*, 14(2):24:1–24:19, July 2018.

[62] Jiating Luo, Cedric Killian, Sebastien Le Beux, Daniel Chillet, Olivier Sentieys, and Ian O'Connor. Offline optimization of wavelength allocation and laser power in nanophotonic interconnects. *J. Emerg. Technol. Comput. Syst.*, 14(2):24:1–24:19, July 2018.

[63] Jiating Luo, Van Dung Pham, Cedric Killian, Daniel Chillet, Sébastien Le Beux, Ian O 'connor, and Olivier Sentieys. POSTER: Wavelength Allocation for Efficient Communications on Optical Network-on-Chip. Conference on Design and Architectures for Signal and Image Processing, October 2016. Poster.

[64] Jiating Luo, Van Dung Pham, Cedric Killian, Daniel Chillet, Ian O'Connor, Olivier Sentieys, and Sebastien Le Beux. Run-time management of energy-performance trade-off in optical network-on-chip. In *XXXIII Conference on Design of Circuits and Integrated Systems*, 14th-16th November 2018.

[65] Jiating Luo, Van Dung Pham, Cedric Killian, Daniel Chillet, Ian O'Connor, Olivier Sentieys, and Sebastien Le Beux. Run-time management of energy-performance trade-off in optical network-on-chip. In *XXXIII Conference on Design of Circuits and Integrated Systems (DCIS), Lyon, France*, November 2018.

[66] D. A. B. Miller. Device requirements for optical interconnects to silicon chips. *Proceedings of the IEEE*, 97(7):1166–1185, July 2009.

[67] T. Mizuochi. Next generation fec for optical communication. In *OFC/NFOEC 2008 - 2008 Conference on Optical Fiber Communication/National Fiber Optic Engineers Conference*, pages 1–33, Feb 2008.

[68] T. Mizuochi, Y. Miyata, T. Kobayashi, K. Ouchi, K. Kuno, K. Kubo, K. Shimizu, H. Tagami, H. Yoshida, H. Fujita, M. Akita, and K. Motoshima. Forward error correction based on block turbo code with 3-bit soft decision for 10-gb/s optical communication systems. *IEEE Journal of Selected Topics in Quantum Electronics*, 10(2):376–386, March 2004.

[69] M. Motoyoshi. Through-silicon via (tsv). *Proceedings of the IEEE*, 97(1):43–48, Jan 2009.

[70] C. T. Nguyen, V. V. Mai, and A. T. Pham. Tcp over free-space optical links with arq and amc: A cross-layer performance analysis. In *2016 International Conference on Advanced Technologies for Communications (ATC)*, pages 80–84, Oct 2016.

[71] M. Nikdast, J. Xu, L. H. K. Duong, X. Wu, X. Wang, Z. Wang, Z. Wang, P. Yang, Y. Ye, and Q. Hao. Crosstalk noise in wdm-based optical networks-on-chip: A formal study and comparison. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 23(11):2552–2565, Nov 2015.

[72] C. Nitta, M. Farrens, and V. Akella. Addressing system-level trimming issues in on-chip nanophotonic networks. In *2011 IEEE 17th International Symposium on High Performance Computer Architecture*, pages 122–131, Feb 2011.

[73] Christopher Nitta. *Design and Analysis of Large Scale Nanophotonic On-Chip Networks*. PhD thesis, University of California, Davis, 2011.

[74] C.J. Nitta, M. Farrens, and V. Akella. *On-Chip Photonic Interconnects: A Computer Architect's Perspective*. Synthesis Lectures on Computer Architecture. Morgan & Claypool Publishers, 2013.

[75] P. Oprisan and B. Bose. Arq in optical networks. In *Proceedings 2001 Pacific Rim International Symposium on Dependable Computing*, pages 251–257, 2001.

[76] Marta Ortin-Obon, Luca Ramini, Victor Vinals, and Davide Bertozzi. Capturing the sensitivity of optical network quality metrics to its network interface parameters. *Concurrency and Computation: Practice and Experience*, 26(15):2504–2517, 2014.

[77] J. D. Owens, W. J. Dally, R. Ho, D. N. Jayasimha, S. W. Keckler, and L. S. Peh. Research challenges for on-chip interconnection networks. *IEEE Micro*, 27(5):96–108, Sept 2007.

[78] Yan Pan, J. Kim, and G. Memik. Flexishare: Channel sharing for an energy-efficient nanophotonic crossbar. In *High Performance Computer Architecture (HPCA), 2010 IEEE 16th International Symposium on*, pages 1–12, Jan 2010.

[79] Yan Pan, Prabhat Kumar, John Kim, Gokhan Memik, Yu Zhang, and Alok Choudhary. Firefly: Illuminating future network-on-chip with nanophotonics. *SIGARCH Comput. Archit. News*, 37(3):429–440, June 2009.

[80] Hyundai Park, Alexander W. Fang, Satoshi Kodama, and John E. Bowers. Hybrid silicon evanescent laser fabricated with a silicon waveguide and iii-v offset quantum wells. *Opt. Express*, 13(23):9460–9464, Nov 2005.

[81] Christophe Peucheret and Dtu Fotonik. Direct & external modulation direct and external modulation of light, 09 2018.

[82] Van Dung Pham, Cédric Killian, Daniel Chillet, Sébastien Le Beux, Olivier Sentieys, and I O 'connor. Gestion de la consommation d'un onoc intégré dans un mpsoc. In *Colloque National du GDR SoC-SiP*, Nantes, France, June 2016.

[83] Van Dung Pham, Cédric Killian, Daniel Chillet, Sébastien Le Beux, Olivier Sentieys, and I O 'connor. Gestion de la consommation d'un réseau optique intégré dans un MPSoC. In *Conférence d'informatique en Parallélisme, Architecture et Système*, Lorient, France, July 2016.

[84] R. Polster, J. L. G. Jimenez, E. Cassan, and L. Vivien. A tia for optical networks-on-chip in 65nm cmos. In *2015 IEEE Optical Interconnects Conference (OI)*, pages 109–110, April 2015.

[85] A. Poorghanad, A. Sadr, and A. Kashanipour. Generating high quality pseudo random number using evolutionary methods. In *2008 International Conference on Computational Intelligence and Security*, volume 1, pages 331–335, Dec 2008.

[86] Proakis. *Digital Communications 5th Edition.* McGraw Hill, 2007.

[87] M. Rakowski, M. Pantouvaki, H. Yu, W. Bogaerts, K. de Meyer, M. Steyaert, B. Snyder, P. O'Brien, J. Ryckaert, P. Absil, and J. Van Campenhout. Low-power, low-penalty, flip-chip integrated, 10gb/s ring-based 1v cmos photonics transmitter. In *2013 Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC)*, pages 1–3, March 2013.

[88] L. Ramini, P. Grani, S. Bartolini, and D. Bertozzi. Contrasting wavelength-routed optical noc topologies for power-efficient 3d-stacked multicore processors using physical-layer analysis. In *2013 Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 1589–1594, March 2013.

[89] I. Reed and G. Solomon. Polynomial codes over certain finite fields. *Journal of the Society for Industrial and Applied Mathematics*, 8(2):300–304, 1960.

[90] IBM Press release. Ibm moves moore's law into the third-dimension. Technical report, International Business Machines, 2007.

[91] IBM Press release. Ibm moves moore's law into the third-dimension. Technical report, International Business Machines, 2010.

[92] A. Rylyakov, C. Schow, B. Lee, W. Green, J. Van Campenhout, M. Yang, F. Doany, S. Assefa, C. Jahnes, J. Kash, and Y. Vlasov. A 3.9ns 8.9mw 4x4 silicon photonic switch hybrid integrated with cmos driver. In *2011 IEEE International Solid-State Circuits Conference*, pages 222–224, Feb 2011.

[93] N. Sadeghi, S. Howard, S. Kasnavi, K. Iniewski, V. C. Gaudet, and C. Schlegel. Analysis of error control code use in ultra-low-power wireless sensor networks. In *2006 IEEE International Symposium on Circuits and Systems*, pages 4 pp.–3561, May 2006.

[94] C. Sciancalepore, B. Ben Bakir, C. Seassal, X. Letartre, J. Harduin, N. Olivier, J. M. Fedeli, and P. Viktorovitch. Thermal, modal, and polarization features of double photonic crystal vertical-cavity surface-emitting lasers. *IEEE Photonics Journal*, 4(2):399–410, April 2012.

[95] J. M. Senior. *Optical Fiber Communications: Principles and Practice*. Pearson Education, 2009.

[96] A. Shacham, K. Bergman, and L. P. Carloni. On the design of a photonic network-on-chip. In *First International Symposium on Networks-on-Chip (NOCS'07)*, pages 53–64, May 2007.

[97] A. Shacham, K. Bergman, and L. P. Carloni. Photonic networks-on-chip for future generations of chip multiprocessors. *IEEE Transactions on Computers*, 57(9):1246–1260, Sept 2008.

[98] Eugene Shih, Seonghwan Cho, Fred S. Lee, Benton H. Calhoun, and Anantha Chandrakasan. Design considerations for energy-efficient radios in wireless microsensor networks. *J. VLSI Signal Process. Syst.*, 37(1):77–94, May 2004.

[99] B. Sklar. *Digital communications: fundamentals and applications*. Prentice Hall Communications Engineering and Emerging Technologies Series. Prentice-Hall PTR, 2001.

[100] Leilei Song, Meng-Lin Yu, and M. S. Shaffer. 10- and 40-gb/s forward error correction devices for optical communications. *IEEE Journal of Solid-State Circuits*, 37(11):1565–1573, Nov 2002.

[101] Xiankai Sun, Avi Zadok, Michael J. Shearn, Kenneth A. Diest, Alireza Ghaffari, Harry A. Atwater, Axel Scherer, and Amnon Yariv. Electrically pumped hybrid evanescent si/ingaasp lasers. *Opt. Lett.*, 34(9):1345–1347, May 2009.

[102] Liang Tang, David A. Miller, Ali K. Okyay, Joseph A. Matteo, Yin Yuen, Krishna C. Saraswat, and Lambertus Hesselink. C-shaped nanoaperture-enhanced germanium photodetector. *Opt. Lett.*, 31(10):1519–1521, May 2006.

[103] Amin Vahdat. Delivering scale out data center networking with optics – why and how. In *Optical Fiber Communication Conference*, page OTu1B.1. Optical Society of America, 2012.

[104] Amin Vahdat, Hong Liu, Xiaoxue Zhao, and Chris Johnson. The emerging optical data center. In *Optical Fiber Communication Conference/National Fiber Optic Engineers Conference 2011*, page OTuH2. Optical Society of America, 2011.

[105] D. Vantrease, R. Schreiber, M. Monchiero, M. McLaren, N.P. Jouppi, M. Fiorentino, A. Davis, N. Binkert, R.G. Beausoleil, and J.H. Ahn. Corona: System implications of emerging nanophotonic technology. In *Computer Architecture, 2008. ISCA '08. 35th International Symposium on*, pages 153–164, June 2008.

[106] M. C. Vuran and I. F. Akyildiz. Cross-layer analysis of error control in wireless sensor networks. In *2006 3rd Annual IEEE Communications Society on Sensor and Ad Hoc Communications and Networks*, volume 2, pages 585–594, Sept 2006.

[107] Jun Wang, Ge Zhang, and Weiwu Hu. An efficient error control scheme for chip-to-chip optical interconnects. In *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pages 3712–3715, May 2007.

[108] Z. Wang, J. Xu, P. Yang, L. H. K. Duong, Z. Wang, X. Wang, Z. Wang, H. Li, and R. K. V. Maeda. A holistic modeling and analysis of optical - electrical interfaces for inter/intra-chip interconnects. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(7):2462–2474, July 2016.

[109] S. Werner, J. Navaridas, and M. Lujan. Amon: An advanced mesh-like optical noc. In *2015 IEEE 23rd Annual Symposium on High-Performance Interconnects*, pages 52–59, Aug 2015.

[110] D. H. Woo, N. H. Seong, D. L. Lewis, and H. H. S. Lee. An optimized 3d-stacked memory architecture by exploiting excessive, high-density tsv bandwidth. In *HPCA - 16 2010 The Sixteenth International Symposium on High-Performance Computer Architecture*, pages 1–12, Jan 2010.

[111] Rui Wu, Chin-Hui Chen, Cheng Li, Tsung-Ching Huang, Fan Lan, Chong Zhang, Yun Pan, John E. Bowers, Raymond G. Beausoleil, and Kwang-Ting Cheng. Variation-aware adaptive tuning for nanophotonic interconnects. In *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, ICCAD '15, pages 487–493, Piscataway, NJ, USA, 2015. IEEE Press.

[112] Xiaowen Wu, Jiang Xu, Yaoyao Ye, Zhehui Wang, Mahdi Nikdast, and Xuan Wang. Suor: Sectioned undirectional optical ring for chip multiprocessor. *J. Emerg. Technol. Comput. Syst.*, 10(4):29:1–29:25, June 2014.

[113] Xiaowen Wu, Jiang Xu, Yaoyao Ye, Zhehui Wang, Mahdi Nikdast, and Xuan Wang. Suor: Sectioned undirectional optical ring for chip multiprocessor. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 10(4):29, 2014.

[114] S. Xiao, M. H. Khan, H. Shen, and M. Qi. Silicon-on-insulator microring add-drop filters with free spectral ranges over 30 nm. *Journal of Lightwave Technology*, 26(2):228–236, Jan 2008.

[115] Shijun Xiao, Maroof H. Khan, Hao Shen, and Minghao Qi. Modeling and measurement of losses in silicon-on-insulator resonators and bends. *Opt. Express*, 15(17):10553–10561, Aug 2007.

[116] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson. 12.5 gbit/s silicon micro-ring silicon modulators. In *2007 Conference on Lasers and Electro-Optics (CLEO)*, pages 1–2, May 2007.

[117] Y. Ye, L. Duan, J. Xu, J. Ouyang, M. K. Hung, and Y. Xie. 3d optical networks-on-chip (noc) for multiprocessor systems-on-chip (mpsoc). In *2009 IEEE International Conference on 3D System Integration*, pages 1–6, Sept 2009.

[118] Yaoyao Ye, Jiang Xu, Xiaowen Wu, Wei Zhang, Weichen Liu, and Mahdi Nikdast. A torus-based hierarchical optical-electronic network-on-chip for multiprocessor system-on-chip. *J. Emerg. Technol. Comput. Syst.*, 8(1):5:1–5:26, February 2012.

[119] Zhiping Zhou, Bing Yin, and Jurgen Michel. On-chip light sources for silicon photonics. *Light: Science &Amp; Applications*, 4:e358 EP –, Nov 2015. Review.

List of Acronyms

3D-IC	Three dimensions integrated circuit
3D-LSI	Three-dimensional large-scale integration
APD	Avalanche Photo-detector
ARQ	Automatic Repeat Request
BER	Bit Error Rate
CMOS	Complementary Metal Oxide Semiconductor
DAG	Directed Acyclic Graph
DES	Deserializer
DWDM	Dense Wavelength Division Multiplexing
ECC	Error Correction Codes
EI	Electrical Interconnects
EMI	Electro-Magnetic Interference
EMU	Energy Management Unit
FC	Fully Connected layer
FDSOI	Fully-Depleted Silicon-On-Insulator
FEC	Forward Error Correction
FIFO	First In First Out
FSR	Free Spectral Range
GF	Galois Field
ITRS	International Technology Road-map for Semiconductors
MMI	Multi-mode Interference
MPSoC	Multiprocessor System-On-Chip
MR	Micro-ring Resonator
MWMR	Multi Writers Multi Readers
MWSR	Multi Writers Single Reader

MWSR	Multiple Writer Single Reader
OCN	Optical Crosstalk Noise
OI	Optical Interconnects
ONI	Optical Network Interface
ONoC	Optical Network On-Chip
OOK	On-Off Keying
OW	Optical Waveguide
PD	Photo-detector
SER	Serializer
SNR	Signal to Noise Ratio
SWMR	Single Writer Multi Readers
SWSR	Single Writer Single Reader
TPA	Two-Photon Absorption
TSV	Through Silicon Via
VCSEL	Vertical-Cavity Surface-Emitting Laser
VLSI	Very-Large-Scale-Integration
WDM	Wavelength Division Multiplexing
WSN	Wireless Sensor Networks

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UNIVERSITE BRETAGNE LOIRE / MATHSTIC

UNIVERSITÉ DE RENNES 1

Titre : Exploration architecturale des interfaces pour les réseaux optiques sur puce efficaces en énergie

Mots clés : réseaux optiques sur puce, interface réseau, codes correcteurs d'erreurs, performance, énergie

Résumé : Depuis quelques années, les réseaux optiques sur puce (ONoC) sont devenus une solution intéressante pour surpasser les limitations des interconnexions électriques, compte tenu de leurs caractéristiques attractives concernant la consommation d'énergie, le délai de transfert et la bande passante. Cependant, les éléments optiques nécessaires pour définir un tel réseau souffrent d'imperfections qui introduisent des pertes durant les communications. De plus, l'utilisation de la technique de multiplexage en longueurs d'ondes (WDM) permet d'augmenter les performances, mais introduit de nouvelles pertes et de la diaphonie entre les longueurs d'ondes, ce qui a pour effet de réduire le rapport signal sur bruit et donc la qualité de la communication. Les contributions présentées dans ce manuscrit adressent cette problématique d'amélioration de performance des liens optiques dans un ONoC.

Pour cela, nous proposons tout d'abord un modèle analytique des pertes et de la diaphonie dans un réseau optique sur puce WDM. Nous proposons ensuite une méthodologie pour améliorer les performances globales du système s'appuyant sur l'utilisation de codes correcteurs d'erreurs. Nous présentons deux types de codes, le premier (Hamming) est d'une complexité d'implémentation faible alors que le second (Reed-Solomon) est plus complexe, mais offre un meilleur taux de correction. Nous avons implémenté des blocs matériels supportant ces corrections d'erreurs avec une technologie 28nm FDSOI. Finalement, nous proposons la définition d'une interface complète entre le domaine électrique et le domaine optique permettant d'allouer les longueurs d'ondes, de coder l'information, de sérialiser le flux de données et de contrôler le driver du laser pour obtenir la modulation à la puissance optique souhaitée.

Title: Architectural Exploration of Network Interface for Energy Efficient 3D Optical Network-on-Chip

Keywords: optical networks on chip, network interface, error correcting codes, performance, energy

Abstract: In recent years, Optical Networks on Chip (ONoC) became an attractive solution to overcome the limitations of current electrical interconnects, thanks to their low power consumption, low latency, and high data bandwidth properties. However, the optical devices used to build ONoCs suffer from some imperfections which introduce losses during communications. Furthermore, Wavelength Division Multiplexing (WDM) technology can further help to improve ONoC's bandwidth and latency. However, using WDM introduces new losses and crosstalk noises which negatively impact the Signal to Noise Ratio and therefore reduces energy efficiency of optical interconnects.

To address these issues, we first provide a model of optical loss and crosstalk in WDM-based ONoC. We then propose a methodology to reduce the power consumption of optical interconnects relying on forward error correction (FEC). We present two case studies of lightweight FEC with low complexity and high error-correction and implement them on a 28nm FDSOI technology. Finally, we propose the complete design of the optical network interface (ONI) composed of allocation and FEC controller, serial to parallel converters, and laser power driver, which creates a runtime allocation management according to application performance and energy requirements.